The ATM Forum
Technical Committee

SSCOP Conformance Abstract Test Suite version 1.1

AF-TEST-0067.001

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Preperation and checking of an abstract test suite of this kind requires the concerted time and effort of many individuals. The Chair wishes to highlight the efforts of the following contributors to this specification:

Leslie Collica

The Chair especially wishes to thank the editor Johan Appelbom for his diligent and extensive work.

Gregan Crawford (Test Working Group Chair)

Contents

1. Introduction

This document provides the conformance abstract test suite for the Service Specific Connection Oriented Protocol (SSCOP) ITU Recommendation Q.2110[2]. This test suite aligns with the principles defined in OSI Conformance Testing Methodology and Framework, ISO 9646 Parts 1-2[3][4]. The test scripts are written in the internationally standardized Tree and Tabular Combined Notation, TTCN, defined in ISO 9646 Part 3[5].

The Protocol Implementation eXtra Information for Testing (PIXIT) proforma is provided in Annex A. The PIXIT questionnaire needs to be completed for a particular System equipment (Implementation Under Test) prior to conformance testing.

1.1 Definition of Terminologies

This test suite uses valid, invalid, and inopportune Protocol Data Units (PDUs) to test the IUT behavior. These terms are defined as follows:

1.1.1 Valid PDU

A valid PDU is an expected PDU which arrives at the correct state or phase and does not belong to any of the categories listed under invalid PDUs.

1.1.2 Invalid PDU

An invalid PDU is a PDU which is syntactically incorrect.

1.1.3 Inopportune PDU

An inopportune PDU is a syntactically valid PDU arriving at a time (IUT's state) when it should be considered irrelevant by the IUT.

1.2 Power Up

Power Up is a function that allows the system to accept a BGN PDU in state Idle irrespectively of the sequence number in the BGN PDU.
This functionality was approved by ITU SG/11 at their plenary January 31,1997. It is described in ITU document COM 11-R 67-E
It is also described by ATMForum contribution 97-0216. ATMForum has accepted this functionality.

2. Methodology

This conformance test suite has been developed as described in ISO/IEC International Standard 9646-1 and 2 [3][4]. A testing matrix has been developed after study of the SSCOP Specification and a selection of the appropriate test groups. The remote single layer embedded (RSE) test method has been selected, as shown below, and test cases have been generated. The notation used in this abstract test suite is the Tree and Tabular Combined Notation (TTCN) as described in ISO/IEC IS 9646-3[5]. This version of the SSCOP conformance test suite uses sequential TTCN, but conversion into concurrent TTCN will bring some improvement in the test case description and implementation.

3. Conformance ATS Status Report

The TTCN of this abstract test suite has passed the syntax checking process for version Af-test-0067.001.mp dated 990219 of the .mp file according to the TTCN specification in ISO 9646 part 3 version ISO/IEC 9646-3:1997 second edition.

STATUS OF TEST SUITE	DATE	COMMENTS
Test suite executed against an implementation	990219	Executed against a simulated environment
Revision	990219	Af-test-0067.001

4. Test Configuration

The test configuration used for testing SSCOP is given in Figure 1. The system under test (SUT) includes the SSCOP of the IUT, the Service Specific Convergence Function (SSCF), and a higher layer, such as Q.2931. For the remote, single layer testing for the SSCOP, the tester has only one Point of Control and Observation (PCO).

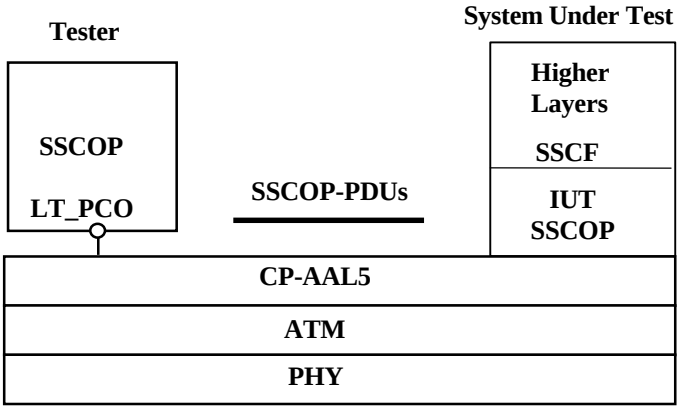

Figure 1. Example Configuration for SSCOP testing using RSE test method

5. Test Suite Structure

For the SSCOP test suite, there are two major groups, Protocol Capabilities (PC) and System Parameters (SP) group. In the PC group, there is a subgroup for each of the SSCOP states (state_x, where x = 1 - 10), each having a subgroup for valid, invalid, and inopportune tests, as defined in the Definitions of Terminologies section above. The System Parameters group includes tests for SSCOP system parameters (e.g., timers and counters).

The test structure for the SSCOP ATS is:

```
- SSCOP/
  - Protocol Capabilities (PC)
      - state_1
            - valid
            - invalid
            - inopportune
      - state_2
            - valid
            - invalid
            - inopportune
      :
      :
      - state_10
            - valid
            - invalid
            - inopportune
- System Parameters (SP)
      - Timer
      - Parm
```

6. Assumptions on the Capabilities of the Testers

6.1 Error Generation

The tester is asked to generate errors in some test cases, to allow for testing of error conditions.

7. Timers

Several timers have been defined for testing. These timers are:

(1) T_Wait is used to limit the test time waiting for "no response" from the IUT.
(2) T_Opr is used to allow sufficient time for a test operator to initiate some test action. This timer is used in conjunction with an "Implicit send" for test coordination.

These timers are not used to verify the exact timing of an implementation, but to limit the time which the test should wait for a PDU or to limit the total duration of the test.

8. Abbreviations

ATM	Asynchronous Transfer Mode
ATS	Abstract Test Suite
ISO/IEC	International Organization for Standardization/International Electrotechnical Commission
IUT	Implementation Under Test
PCO	Point of Control and Observation
PDU	Protocol Data Unit
PHY	Physical Layer
PICS	Protocol Implementation Conformance Statement
PIXIT	Protocol Implementation Extra Information for Testing
RSE	Remote Single Layer Embedded test method
SSCF	Service Specific Convergence Function
SSCOP	Service Specific Connection Oriented Protocol
SUT	System Under Test
TTCN	Tree and Tabular Combined Notation
UNI	User-Network Interface

9. References

[1] ATM Forum User-Network Interface (UNI) Specification 3.1.

[2] ITU Recommendation Q.2110, B-*ISDN - ATM Adaptation Layer - Service Specific Connection Oriented Protocol (SSCOP).*

[3] ISO/IEC 9646-1 *"Information Technology - Open Systems Interconnection - Conformance testing methodology and framework - Part 1: General Concepts", 1991.*

[4] ISO/IEC 9646-2 *"Information Technology - Open Systems Interconnection - Conformance testing methodology and framework - Part 2: Abstract test suite specification", 1991.*

[5] ISO/IEC 9646-3 *"Information Technology - Open Systems Interconnection - Conformance testing methodology and framework - Part 3: The tree and tabular combined notation", 1991.*

Annex A PIXIT

Protocol Implementation eXtra Information for Testing (PIXIT) Proforma For SSCOP

IUT

Name:

Version:

Machine Configuration:

Operating System Identification:

IUT Identification:

PICS Reference for IUT:

Limitations of the IUT :

Timers

Item #	Question	Value	Answer
T1	Enter the value for the timer that is used when no response is expected from the IUT(T_Wait).	ms	
T2	Enter the value for the timer that is long enough to allow test operator intervention (T_Opr).	s	

General

Item #	Question	Answer(Yes/No)
G1	Can the IUT, at state 1, be forced to send BGN PDU when requested by test operator?	
G2	Can the IUT, at state 4, be forced to send BGN PDU when requested by test operator?	
G3	Can the IUT, at state 2, be forced to send END PDU when requested by test operator?	
G4	Can the IUT, at state 5, be forced to send END PDU when requested by test operator?	
G5	Can the IUT, at state 10, be forced to send END PDU when requested by test operator?	
G6	Can the IUT, at state 10, be forced to send RS PDU when requested by test operator?	
G7	Can the IUT, at state 10, be forced to send POLL PDU when requested by test operator?	
G8	Can the IUT, at state 10, be forced to send SD PDU when requested by test operator?	

Power Up

Item #	Question	Test Suite parameter name	Answer (Yes/No)
PU1	Is Power up implemented?	Power_up_robust	

Annex B Abstract Test Suite

Abstract Test Suite

af_test_0067_001

Mon Feb 22 17:16:09 1999

I

Test Suite Overview

Test Suite Structure

Suite Name : af_test_0067_001

Standards Ref: ITU−T Recommendation Q.2110, Service Specific Connection Oriented Protocol(SSCOP)

PICS Ref : ITU−T Recommendation Q.2110, Annex B

PIXIT Ref : ATM Forum/af−test−0067.001, Conformance ATS for SSCOP, Annex A

Test Method(s): Remote Single Layer Embedded Test Method

Comments :

Test Group Reference	Selection Ref	Test Group Objective	Page Nr
PC/		Protocol Capabilities	
PC/STATE_1/			
PC/STATE_1/VAL/			
PC/STATE_1/INV/			
PC/STATE_1/INOP/			
PC/STATE_2/			
PC/STATE_2/VAL/			
PC/STATE_2/INV/			
PC/STATE_4/			
PC/STATE_4/VAL/			
PC/STATE_4/INV/			
PC/STATE_5/			
PC/STATE_5/VAL/			
PC/STATE_5/INV/			
PC/STATE_5/INOP/			
PC/STATE_7/			
PC/STATE_7/VAL/			
PC/STATE_7/INV/			
PC/STATE_7/INOP/			
PC/STATE_10/			
PC/STATE_10/VAL/			
PC/STATE_10/INV/			
PC/STATE_10/INOP/			
SP/		System Parameters	
SP/TIMER_TESTS/			
SP/PARAM/			

Detailed Comments:

Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_1/VAL/	S1_V_A1		Verify that the IUT generates the BGN PDU on demand at state 1.	
PC/STATE_1/VAL/	S1_V_P1		Verify that the IUT goes to state 3, if power−up robustness is implemented, or sends a BGREJ PDU, if not , on reception of retransmitted BGN PDU.	
PC/STATE_1/VAL/	S1_V_P2		Verify that the IUT goes to state 3 on reception of BGN PDU at state 1.	
PC/STATE_1/VAL/	S1_V_P5		Verify that the IUT sends a ENDAK PDU on reception of a END PDU at state 1.	
PC/STATE_1/VAL/	S1_V_P6		Verify that the IUT ignores a ENDAK PDU and remains at state 1.	
PC/STATE_1/VAL/	S1_V_P16		Verify that the IUT accpets a UD PDU at state 1.	
PC/STATE_1/VAL/	S1_V_P17		Verify that the IUT accpets a MD PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I1		Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 1.	
PC/STATE_1/INV/	S1_IV_I2		Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 1.	
PC/STATE_1/INV/	S1_IV_I3		Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 1.	
PC/STATE_1/INV/	S1_IV_I4		Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 1.	
PC/STATE_1/INV/	S1_IV_I6		Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 1.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_1/INV/	S1_IV_I10		Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 1.	
PC/STATE_1/INV/	S1_IV_I14		Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 1.	
PC/STATE_1/INV/	S1_IV_I15		Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 1.	
PC/STATE_1/INV/	S1_IV_I16		Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I17		Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I18		Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I19		Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I20_1		Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 1.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_1/INV/	S1_IV_I20_2		Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I21		Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I22_1		Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I22_2		Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I23_1		Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I23_2		Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I24_1		Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 1.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_1/INV/	S1_IV_I24_2		Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I25		Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I26_1		Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I26_2		Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I27_1		Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I27_2		Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I28_1		Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 1.	

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_1/INV/	S1_IV_I28_2		Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTAT PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I29		Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I30		Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 1.	
PC/STATE_1/INV/	S1_IV_I31		Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 1.	
PC/STATE_1/INOP/	S1_IO_P3		Verify that the IUT sends a END PDU on reception of a BGAK PDU at state 1.	
PC/STATE_1/INOP/	S1_IO_P4		Verify that the IUT ignores a BGREJ PDU and remains at state 1.	
PC/STATE_1/INOP/	S1_IO_P8		Verify that the IUT sends a END PDU on reception of a RS PDU at state 1.	
PC/STATE_1/INOP/	S1_IO_P9		Verify that the IUT sends a END PDU on reception of a RSAK PDU at state 1.	
PC/STATE_1/INOP/	S1_IO_P10		Verify that the IUT sends a END PDU on reception of a ER PDU at state 1.	
PC/STATE_1/INOP/	S1_IO_P11		Verify that the IUT sends a END PDU on reception of a ERAK PDU at state 1.	
PC/STATE_1/INOP/	S1_IO_P12		Verify that the IUT sends a END PDU on reception of a SD PDU at state 1.	

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_1/INOP/	S1_IO_P13		Verify that the IUT sends a END PDU on reception of a POLL PDU at state 1.	
PC/STATE_1/INOP/	S1_IO_P14		Verify that the IUT sends a END PDU on reception of a STAT PDU at state 1.	
PC/STATE_1/INOP/	S1_IO_P15		Verify that the IUT sends a END PDU on reception of a USTAT PDU at state 1.	
PC/STATE_2/VAL/	S2_V_A3		Verify that the IUT generates the END PDU on demand at state 2.	
PC/STATE_2/VAL/	S2_V_P1		Verify that the IUT ignores a retransmitted BGN PDU at state 2.	
PC/STATE_2/VAL/	S2_V_P2		Verify that the IUT sends a BGAK PDU on reception of BGN PDU and goes to state 10.	
PC/STATE_2/VAL/	S2_V_P3		Verify that the IUT goes to state 10 on reception of BGAK PDU at state 2.	
PC/STATE_2/VAL/	S2_V_P4		Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 2.	
PC/STATE_2/VAL/	S2_V_P5		Verify that the IUT ignores a END PDU and remains at state 2.	
PC/STATE_2/VAL/	S2_V_P6		Verify that the IUT ignores a ENDAK PDU and remains at state 2.	
PC/STATE_2/VAL/	S2_V_P8		Verify that the IUT ignores a RS PDU and remains at state 2.	
PC/STATE_2/VAL/	S2_V_P9		Verify that the IUT ignores a RSAK PDU and remains at state 2.	
PC/STATE_2/VAL/	S2_V_P10		Verify that the IUT ignores a ER PDU and remains at state 2.	

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_2/VAL/	S2_V_P11		Verify that the IUT ignores a ERAK PDU and remains at state 2.	
PC/STATE_2/VAL/	S2_V_P12		Verify that the IUT ignores a SD PDU and remains at state 2.	
PC/STATE_2/VAL/	S2_V_P13		Verify that the IUT ignores a POLL PDU and remains at state 2.	
PC/STATE_2/VAL/	S2_V_P14		Verify that the IUT ignores a STAT PDU and remains at state 2.	
PC/STATE_2/VAL/	S2_V_P15		Verify that the IUT ignores a USTAT PDU and remains at state 2.	
PC/STATE_2/VAL/	S2_V_P16		Verify that the IUT accpets a UD PDU at state 2.	
PC/STATE_2/VAL/	S2_V_P17		Verify that the IUT accpets a MD PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I1		Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 2.	
PC/STATE_2/INV/	S2_IV_I2		Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 2.	
PC/STATE_2/INV/	S2_IV_I3		Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 2.	
PC/STATE_2/INV/	S2_IV_I4		Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 2.	
PC/STATE_2/INV/	S2_IV_I6		Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 2.	
PC/STATE_2/INV/	S2_IV_I10		Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 2.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_2/INV/	S2_IV_I14		Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 2.	
PC/STATE_2/INV/	S2_IV_I15		Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 2.	
PC/STATE_2/INV/	S2_IV_I16		Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I17		Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I18		Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I19		Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I20_1		Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I20_2		Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 2.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_2/INV/	S2_IV_I21		Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I22_1		Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I22_2		Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I23_1		Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I23_2		Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I24_1		Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I24_2		Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 2.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_2/INV/	S2_IV_I25		Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I26_1		Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I26_2		Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I27_1		Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I27_2		Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I28_1		Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I28_2		Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTAT PDU at state 2.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_2/INV/	S2_IV_I29		Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I30		Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 2.	
PC/STATE_2/INV/	S2_IV_I31		Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 2.	
PC/STATE_4/VAL/	S4_V_A1		Verify that the IUT generates the BGN PDU on demand at state 4.	
PC/STATE_4/VAL/	S4_V_P1		Verify that the IUT sends a BGAK and END PDU on reception of retransmitted BGN PDU at state 4.	
PC/STATE_4/VAL/	S4_V_P2		Verify that the IUT goes to state 3 on reception of BGN PDU at state 4.	
PC/STATE_4/VAL/	S4_V_P3		Verify that the IUT ignores a BGAK PDU and remains at state 4.	
PC/STATE_4/VAL/	S4_V_P4		Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 4.	
PC/STATE_4/VAL/	S4_V_P5		Verify that the IUT sends a ENDAK PDU on reception of a END PDU at state 4.	
PC/STATE_4/VAL/	S4_V_P6		Verify that the IUT goes to state 1 on reception of ENDAK PDU at state 4.	
PC/STATE_4/VAL/	S4_V_P8		Verify that the IUT ignores a RS PDU and remains at state 4.	
PC/STATE_4/VAL/	S4_V_P9		Verify that the IUT ignores a RSAK PDU and remains at state 4.	

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_4/VAL/	S4_V_P10		Verify that the IUT ignores a ER PDU and remains at state 4.	
PC/STATE_4/VAL/	S4_V_P11		Verify that the IUT ignores a ERAK PDU and remains at state 4.	
PC/STATE_4/VAL/	S4_V_P12		Verify that the IUT ignores a SD PDU and remains at state 4.	
PC/STATE_4/VAL/	S4_V_P13		Verify that the IUT ignores a POLL PDU and remains at state 4.	
PC/STATE_4/VAL/	S4_V_P14		Verify that the IUT ignores a STAT PDU and remains at state 4.	
PC/STATE_4/VAL/	S4_V_P15		Verify that the IUT ignores a USTAT PDU and remains at state 4.	
PC/STATE_4/VAL/	S4_V_P16		Verify that the IUT accpets a UD PDU at state 4.	
PC/STATE_4/VAL/	S4_V_P17		Verify that the IUT accpets a MD PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I1		Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 4.	
PC/STATE_4/INV/	S4_IV_I2		Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 4.	
PC/STATE_4/INV/	S4_IV_I3		Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 4.	
PC/STATE_4/INV/	S4_IV_I4		Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 4.	
PC/STATE_4/INV/	S4_IV_I6		Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 4.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_4/INV/	S4_IV_I10		Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 4.	
PC/STATE_4/INV/	S4_IV_I14		Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 4.	
PC/STATE_4/INV/	S4_IV_I15		Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 4.	
PC/STATE_4/INV/	S4_IV_I16		Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I17		Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I18		Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I19		Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I20_1		Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 4.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_4/INV/	S4_IV_I20_2		Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I21		Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I22_1		Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I22_2		Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I23_1		Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I23_2		Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I24_1		Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 4.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_4/INV/	S4_IV_I24_2		Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I25		Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I26_1		Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I26_2		Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I27_1		Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I27_2		Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I28_1		Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 4.	

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_4/INV/	S4_IV_I28_2		Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTAT PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I29		Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I30		Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 4.	
PC/STATE_4/INV/	S4_IV_I31		Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 4.	
PC/STATE_5/VAL/	S5_V_A3		Verify that the IUT generates the END PDU on demand at state 5.	
PC/STATE_5/VAL/	S5_V_P1		Verify that the IUT sends a BGAK and RS PDU on reception of retransmitted BGN PDU at state 5.	
PC/STATE_5/VAL/	S5_V_P2		Verify that the IUT goes to state 3 on reception of BGN PDU at state 5	
PC/STATE_5/VAL/	S5_V_P3		Verify that the IUT ignores a BGAK PDU and remains at state 5.	
PC/STATE_5/VAL/	S5_V_P5		Verify that the IUT sends a ENDAK PDU on reception of a END PDU at state 5.	
PC/STATE_5/VAL/	S5_V_P7		Verify that the IUT ignores a retransmitted RS PDU and remains at state 5.	

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_5/VAL/	S5_V_P8		Verify that the IUT sends a RSAK PDU on reception of RS PDU and goes to state 10.	
PC/STATE_5/VAL/	S5_V_P9		Verify that the IUT goes to state 10 on reception of RSAK PDU at state 5.	
PC/STATE_5/VAL/	S5_V_P10		Verify that the IUT ignores a ER PDU and remains at state 5.	
PC/STATE_5/VAL/	S5_V_P11		Verify that the IUT ignores a ERAK PDU and remains at state 5.	
PC/STATE_5/VAL/	S5_V_P12		Verify that the IUT ignores a SD PDU and remains at state 5.	
PC/STATE_5/VAL/	S5_V_P13		Verify that the IUT ignores a POLL PDU and remains at state 5.	
PC/STATE_5/VAL/	S5_V_P14		Verify that the IUT ignores a STAT PDU and remains at state 5.	
PC/STATE_5/VAL/	S5_V_P15		Verify that the IUT ignores a USTAT PDU and remains at state 5.	
PC/STATE_5/VAL/	S5_V_P16		Verify that the IUT accpets a UD PDU at state 5.	
PC/STATE_5/VAL/	S5_V_P17		Verify that the IUT accpets a MD PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I1		Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 5.	
PC/STATE_5/INV/	S5_IV_I2		Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 5.	
PC/STATE_5/INV/	S5_IV_I3		Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 5.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_5/INV/	S5_IV_I4		Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 5.	
PC/STATE_5/INV/	S5_IV_I6		Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 5.	
PC/STATE_5/INV/	S5_IV_I10		Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 5.	
PC/STATE_5/INV/	S5_IV_I14		Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 5.	
PC/STATE_5/INV/	S5_IV_I15		Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 5.	
PC/STATE_5/INV/	S5_IV_I16		Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I17		Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I18		Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I19		Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 5.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_5/INV/	S5_IV_I20_1		Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I20_2		Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I21		Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I22_1		Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I22_2		Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I23_1		Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I23_2		Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 5.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_5/INV/	S5_IV_I24_1		Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I24_2		Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I25		Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I26_1		Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I26_2		Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I27_1		Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I27_2		Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 5.	

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_5/INV/	S5_IV_I28_1		Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I28_2		Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTAT PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I29		Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I30		Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 5.	
PC/STATE_5/INV/	S5_IV_I31		Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 5.	
PC/STATE_5/INOP/	S5_IO_P4		Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 5.	
PC/STATE_5/INOP/	S5_IO_P6		Verify that the IUT goes to state 1 on reception of ENDAK PDU at state 5.	
PC/STATE_7/VAL/	S7_V_P2		Verify that the IUT goes to state 3 on reception of BGN PDU at state 7.	
PC/STATE_7/VAL/	S7_V_P5		Verify that the IUT sends a ENDAK PDU and goes to state 1 on reception of a END PDU at state 7.	
PC/STATE_7/VAL/	S7_V_P8		Verify that the IUT goes to state 6 on reception of RS PDU at state 7.	

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_7/VAL/	S7_V_P11		Verify that the IUT sends a ERAK PDU and goes to state 8 on reception of a ER PDU at state 7.	
PC/STATE_7/VAL/	S7_V_P12		Verify that the IUT goes to state 8 on reception of ERAK PDU at state 7.	
PC/STATE_7/VAL/	S7_V_P19		Verify that the IUT ignores a SD PDU and remains at state 7.	
PC/STATE_7/VAL/	S7_V_P21		Verify that the IUT ignores a POLL PDU and remains at state 7.	
PC/STATE_7/VAL/	S7_V_P26		Verify that the IUT ignores a STAT PDU and remains at state 7.	
PC/STATE_7/VAL/	S7_V_P36		Verify that the IUT ignores a USTAT PDU and remains at state 7.	
PC/STATE_7/VAL/	S7_V_P40		Verify that the IUT accpets a UD PDU at state 7.	
PC/STATE_7/VAL/	S7_V_P41		Verify that the IUT accpets a MD PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I1		Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 7.	
PC/STATE_7/INV/	S7_IV_I2		Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 7.	
PC/STATE_7/INV/	S7_IV_I3		Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 7.	
PC/STATE_7/INV/	S7_IV_I4		Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 7.	
PC/STATE_7/INV/	S7_IV_I6		Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 7.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_7/INV/	S7_IV_I10		Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 7.	
PC/STATE_7/INV/	S7_IV_I14		Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 7.	
PC/STATE_7/INV/	S7_IV_I15		Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 7.	
PC/STATE_7/INV/	S7_IV_I16		Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I17		Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I18		Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I19		Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I20_1		Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 7.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_7/INV/	S7_IV_I20_2		Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I21		Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I22_1		Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I22_2		Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I23_1		Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I23_2		Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I24_1		Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 7.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_7/INV/	S7_IV_I24_2		Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I25		Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I26_1		Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I26_2		Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I27_1		Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I27_2		Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I28_1		Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 7.	

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_7/INV/	S7_IV_I28_2		Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTAT PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I29		Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I30		Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 7.	
PC/STATE_7/INV/	S7_IV_I31		Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 7.	
PC/STATE_7/INOP/	S7_IO_P1		Verify that the IUT ignores a retransmitted BGN PDU and remains at state 7.	
PC/STATE_7/INOP/	S7_IO_P3		Verify that the IUT ignores a BGAK PDU and remains at state 7.	
PC/STATE_7/INOP/	S7_IO_P4		Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 7.	
PC/STATE_7/INOP/	S7_IO_P6		Verify that the IUT goes to state 1 on reception of ENDAK PDU at state 7.	
PC/STATE_7/INOP/	S7_IO_P7		Verify that the IUT ignores a retransmitted RS PDU and remains at state 7.	
PC/STATE_7/INOP/	S7_IO_P9		Verify that the IUT ignores a RSAK PDU and remains at state 7.	
PC/STATE_7/INOP/	S7_IO_P10		Verify that the IUT ignores a retransmitted ER PDU and remains at state 7.	

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Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_10/VAL/	S10_V_A3		Verify that the IUT, at state 10, generates the END PDU on demand.	
PC/STATE_10/VAL/	S10_V_A5		Verify that the IUT, at state 10, generates the RS PDU on demand.	
PC/STATE_10/VAL/	S10_V_P1		Verify that the IUT, at state 10, sends a BGAK PDU on reception of a retransmitted BGN PDU.	
PC/STATE_10/VAL/	S10_V_P2		Verify that the IUT, at state 10, goes to state 3 on reception of BGN PDU.	
PC/STATE_10/VAL/	S10_V_P3		Verify that the IUT, at state 10, ignores a BGAK PDU and remains.	
PC/STATE_10/VAL/	S10_V_P5		Verify that the IUT, at state 10, sends a ENDAK PDU and goes to state 1 on reception of a END PDU.	
PC/STATE_10/VAL/	S10_V_P7		Verify that the IUT, at state 10, sends a RSAK PDU on reception of a retransmitted RS PDU.	
PC/STATE_10/VAL/	S10_V_P8		Verify that the IUT, at state 10, goes to state 6 on reception of RS PDU.	
PC/STATE_10/VAL/	S10_V_P9		Verify that the IUT, at state 10, ignores a RSAK PDU and remains.	
PC/STATE_10/VAL/	S10_V_P10		Verify that the IUT, at state 10, sends a ERAK PDU on reception of a retransmitted ER PDU.	
PC/STATE_10/VAL/	S10_V_P11		Verify that the IUT, at state 10, goes to state 9 on reception of ER PDU.	
PC/STATE_10/VAL/	S10_V_P12		Verify that the IUT, at state 10, ignores a ERAK PDU and remains.	
PC/STATE_10/VAL/	S10_V_P13		Verify that the IUT, at state 10, sends a USTAT PDU on reception of SD PDU out of the window.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_10/VAL/	S10_V_P14		Verify that the IUT, at state 10, ignores a SD PDU that is out of the window when window is not available.	
PC/STATE_10/VAL/	S10_V_P15		Verify that the IUT, at state 10, saves the next highest expected SD PDU.	
PC/STATE_10/VAL/	S10_V_P17		Verify that the IUT, at state 10, saves a SD PDU that sequence number is between the sequence number of the next in sequence and the next highest expected SD PDU.	
PC/STATE_10/VAL/	S10_V_P18		Verify that the IUT, at state 10, sends a ER PDU on reception of a SD PDU that sequence number is between the sequence number of the next in sequence and the next highest expected SD PDUs and is already in RX BUFFER.	
PC/STATE_10/VAL/	S10_V_P19		Verify that the IUT, at state 10, accepts the next in sequence SD PDU.	
PC/STATE_10/VAL/	S10_V_P21		Verify that the IUT, at state 10, sends a ER PDU on reception of a POLL PDU that sequence number is less than that of the next highest expected SD PDU.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_10/VAL/	S10_V_P22		Verify that the IUT, at state 10, sends a STAT PDU on reception of a POLL PDU that sequence number is greater than that of the next highest expected SD PDU and is out of the window.	
PC/STATE_10/VAL/	S10_V_P23_1		Verify that the IUT, at state 10, sends a STAT PDU on reception of a POLL PDU that sequence number is greater than that of the next highest expected SD PDU and is out of the window.	
PC/STATE_10/VAL/	S10_V_P23_2		Verify that the IUT, at state 10, sends a STAT PDUs(with segmenting) on reception of a POLL PDU that sequence number is greater than that of the next highest expected SD PDU and is out of the window.	
PC/STATE_10/VAL/	S10_V_P24		Verify that the IUT, at state 10 and having no missing gap of received SD PDUs, sends a STAT PDU on reception of a POLL PDU that sequence number is less than or equal to that of the next highest expected SD PDU and is within the window.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_10/VAL/	S10_V_P25		Verify that the IUT, at state 10 and having a missing gap of received SD PDUs, sends a STAT PDU on reception of a POLL PDU that sequence number is less than or equal to that of the next highest expected SD PDU and is within the window.	
PC/STATE_10/VAL/	S10_V_P26		Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number is incorrect.	
PC/STATE_10/VAL/	S10_V_P27		Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number is correct but SD PDU sequence number is incorrect.	
PC/STATE_10/VAL/	S10_V_P32		Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number and SD PDU sequence number are correct but its list element has incorrect sequence number.	
PC/STATE_10/VAL/	S10_V_P33		Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number and SD PDU sequence number are correct but its list elements are not increasing order.	

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Continued from previous page

Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_10/VAL/	S10_V_P38_1		Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a USTAT PDU that list element has incorrect sequence number.	
PC/STATE_10/VAL/	S10_V_P38_2		Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a USTAT PDU that list elements are not increasing order.	
PC/STATE_10/VAL/	S10_V_P39		Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a USTAT PDU that list elements are not increasing order.	
PC/STATE_10/VAL/	S10_V_P40		Verify that the IUT accpets a UD PDU at state 10.	
PC/STATE_10/VAL/	S10_V_P41		Verify that the IUT accpets a MD PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I1		Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 10.	
PC/STATE_10/INV/	S10_IV_I2		Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 10.	
PC/STATE_10/INV/	S10_IV_I3		Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 10.	
PC/STATE_10/INV/	S10_IV_I4		Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 10.	
PC/STATE_10/INV/	S10_IV_I6		Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 10.	

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Test Case Index

Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_10/INV/	S10_IV_I10		Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 10.	
PC/STATE_10/INV/	S10_IV_I14		Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 10.	
PC/STATE_10/INV/	S10_IV_I15		Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 10.	
PC/STATE_10/INV/	S10_IV_I16		Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I17		Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I18		Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I19		Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I20_1		Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 10.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_10/INV/	S10_IV_I20_2		Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I21		Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I22_1		Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I22_2		Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I23_1		Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I23_2		Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I24_1		Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 10.	

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Continued from previous page

Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_10/INV/	S10_IV_I24_2		Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I25		Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I26_1		Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I26_2		Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I27_1		Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I27_2		Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I28_1		Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 10.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
PC/STATE_10/INV/	S10_IV_I28_2		Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTAT PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I29		Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I30		Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 10.	
PC/STATE_10/INV/	S10_IV_I31		Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 10.	
PC/STATE_10/INOP/	S10_IO_P4		Verify that the IUT, at state 10, goes to state 1 on reception of BGREJ PDU.	
PC/STATE_10/INOP/	S10_IO_P6		Verify that the IUT, at state 10, goes to state 1 on reception of ENDAK PDU.	
SP/TIMER_TESTS/	S2_CC_T1		Verify that the IUT, at state 2, sends a END PDU and goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.	
SP/TIMER_TESTS/	S4_CC_T1		Verify that the IUT, at state 4, goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.	

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Test Case Index				
Test Group Reference	Test Case Id	Selection Ref	Description	Page Nr
SP/TIMER_TESTS/	S5_CC_T1		Verify that the IUT, at state 5, sends a END PDU and goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.	
SP/TIMER_TESTS/	S7_CC_T1		Verify that the IUT, at state 7, sends a END PDU and goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.	
SP/TIMER_TESTS/	S10_POLL_T3		Verify that the IUT, at state 10, sends a POLL PDU when the Timer Timer_POLL is expired.	
SP/TIMER_TESTS/	S10_KEEP_ALIVE_T4		Verify that the IUT, at state 10, sends a POLL PDU when the Timer Timer_KEEP_ALIVE is expired.	
SP/TIMER_TESTS/	S10_IDLE_T5		Verify that the IUT, at state 10, sends a POLL PDU when the Timer Timer_IDLE is expired.	
SP/TIMER_TESTS/	S10_NO_RESPONSE_T6		Verify that the IUT, at state 10, sends a END PDU when the Timer Timer_NO_RESPONSE is expired.	
SP/PARAM/	SP3_MaxPD		Check the value of MaxPD system parameter(Maximum number of SD PDUs before transmission of a POLL PDU).	
Detailed Comments				

Test Step Index

Test Step Group Reference	Test Step Id	Description	Page Nr
GENERAL/	TS_Wait	Test Step of alternatives OTHERWISE, and TIMEOUT of T_Wait.	
GENERAL/	TS_Opr	Test Step of alternatives OTHERWISE, and TIMEOUT of T_Opr.	
GENERAL/	TS_CC	Test Step of alternatives OTHERWISE, and TIMEOUT of Timer_CC.	
GENERAL/	RESTORE_SEQUENCE		
PROCEDURE/	Initialize_State_Variables	Procedure used to initialize state variables when new connection is established.	
	postamble	Procedure used to place the IUT at state 1.	
PREAMBLE/	S1_PREAMBLE	Procedure used to place the IUT at state 1 from any state.	
PREAMBLE/	S2_PREAMBLE	Procedure used to place the IUT at state 2 from any state.	
PREAMBLE/	S4_PREAMBLE	Procedure used to place the IUT at state 4 from any state.	
PREAMBLE/	S5_PREAMBLE	Procedure used to place the IUT at state 5 from any state.	
PREAMBLE/	S7_PREAMBLE	Procedure used to place the IUT at state 7 from any state.	
PREAMBLE/	S10_PREAMBLE	Procedure used to place the IUT at state 10 from any state.	
VERIFY/	S1_VERIFY	Procedure used to verify that the IUT is at state 1.	
VERIFY/	S2_VERIFY	Procedure used to verify that the IUT is at state 2.	
VERIFY/	S4_VERIFY	Procedure used to verify that the IUT is at state 4.	
VERIFY/	S5_VERIFY	Procedure used to verify that the IUT is at state 5.	
VERIFY/	S7_VERIFY	Procedure used to verify that the IUT is at state 7.	
VERIFY/	S10_VERIFY	Procedure used to verify that the IUT is at state 10.	

Detailed Comments

II

Declarations Part

ASN.1 Type Definition
Type Name : LIST_ELEMENT_TYPE Encoding Variation Comments : Used for STAT PDU Type definition
Type Definition

SEQUENCE {
pAD OCTET STRING(SIZE (1..1)),
IE BIT STRING(SIZE (24..24))
}

Detailed Comments

ASN.1 Type Definition
Type Name : LIST_TYPE Encoding Variation Comments : Used for STAT PDU Type definition
Type Definition
SEQUENCE OF LIST_ELEMENT_TYPE
Detailed Comments

Test Suite Operation Definition
Operation Name: GET_VR_MR Result Type : INTEGER Comments :
Description
This operation is used to set the Maximum acceptable Receive state value(VR(MR)). Updating VR(MR) is implementation dependent, but VR(MR) should not be set to a value < VR(H). An example of how VR)MR) may be determined is included in Appendix IV of Recommendation Q.2110.
Detailed Comments

Test Suite Operation Definition
Operation Name: APPEND_LIST(parLIST:LIST_TYPE;parLE:INTEGER) Result Type : LIST_TYPE Comments :
Description
This operation is used to append new element of value "parLE" to existing list "parLIST". The procedures of this operation is as follows: 1. Make a instance of LIST_ELEMENT_TYPE which has "00"O as PAD field and bitstring of encoded value of "parLE" as LE field. 2. Append the instance of above to existing list of "parLIST". 3. Return the new list.
Detailed Comments

Test Suite Operation Procedural Definition
Operation Name: CHECK_N_PS(parPA,parN_PS,parPS:INTEGER) Result Type : BOOLEAN Comments : This operation is used to check if the value of parameter "N(PS)" in STAT PDU is valid or not.
Description

VAR
LV_parPA:INTEGER:parPA;
LV_parN_PS:INTEGER:parN_PS;
LV_parPS:INTEGER:parPS;
LV_returnvalue:BOOLEAN;
ENDVAR
BEGIN
IF (LV_parPA<=LV_parN_PS)
THEN
IF (LV_parN_PS<=LV_parPS)
THEN
LV_returnvalue:= TRUE;
ELSE
LV_returnvalue:= FALSE;
ENDIF;
ELSE
LV_returnvalue:= FALSE;
ENDIF;
RETURNVALUE LV_returnvalue;
END

Detailed Comments

Test Suite Operation Procedural Definition
Operation Name: INC_MOD_8(parIN, amount:INTEGER) Result Type : INTEGER Comments : INC_MOD_8(parIN, amount) is the modulo incremented value of "parIN" in the amount of "amount". The modulus equals 2E8(256). For example: INC_MOD_8(3,4)=7 INC_MOD_8(255,1)=0
Description
VAR LV_parIN:INTEGER:parIN; LV_amount:INTEGER:amount; LV_returnvalue:INTEGER; ENDVAR BEGIN LV_returnvalue:=(LV_parIN + LV_amount) MOD 256; RETURNVALUE LV_returnvalue; END
Detailed Comments

Test Suite Operation Procedural Definition
Operation Name: INC_MOD_24(parIN, amount:INTEGER) Result Type : INTEGER Comments : INC_MOD_24(parIN, amount) is the modulo incremented value of "parIN" in the amount of "amount". The modulus equals 2E8(16777216). For example: INC_MOD_24(3,4)=7 INC_MOD_24(16777215,1)=0
Description
VAR LV_parIN:INTEGER:parIN; LV_amount:INTEGER:amount; LV_returnvalue:INTEGER; ENDVAR BEGIN LV_returnvalue:=(LV_parIN + LV_amount) MOD 16777216; RETURNVALUE LV_returnvalue; END
Detailed Comments

Test Suite Parameter Declarations			
Parameter Name	Type	PICS/PIXIT Ref	Comments
Max_CC	INTEGER	PICS SP1	Maximum Number of transmissions of a BGN, END, ER, or RS PDU(MaxCC)
Max_PD	INTEGER	PICS SP2	Maximum Number of SD PDUs before transmission of a POLL PDU(MaxPD)
Max_STAT	INTEGER	PICS SP3	Maximum Number of list elements placed in a STAT PDU
TimerPOLLtime	INTEGER	PICS SP5	The time between transmission of POLL PDU at active phase
TimerKEEP_ALIVEtime	INTEGER	PICS SP6	The time between transmission of POLL PDU at transient phase
TimerNO_RESPONSEtime	INTEGER	PICS SP7	The maximum time interval during which at least one STAT PDU needs to be received.
TimerIDLEtime	INTEGER	PICS SP8	may be considerably greater than Timer_KEEP_ALIVE
TimerCCtime	INTEGER	PICS SP9	The time between transmission of BGN, END, ER, or RS PDU
Power_up_robust	BOOLEAN	PIXIT PU1	True if the IUT has power−up robustness implemented
WAITtime	INTEGER	PIXIT T1	Used to limit the test time waiting for "no response" from the IUT
TESTtime	INTEGER	PIXIT T2	The value for the timer that is long enough to allow test operator intervention
UU_Max_Len	INTEGER	PICS SP10	PICS SP10 − Maximum length of variable length SSCOP−UU field
Info_Max_Len	INTEGER	PICS SP4	PICS SP4 − The maximum length of information field in SD, UD, MD PDUs. This value may be derived from the maximum langth PDU size. (Info_Max_Len = PICS SP4 − 4)

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Test Suite Parameter Declarations			
Parameter Name	Type	PICS/PIXIT Ref	Comments
ST1_BGN	BOOLEAN	PIXIT G1	Can the IUT send a BGN−PDU on request in state 1?
ST4_BGN	BOOLEAN	PIXIT G2	Can the IUT send a BGN−PDU on request at state 4?
ST2_END	BOOLEAN	PIXIT G3	Can the IUT send an END−PDU on request at state 2?
ST5_END	BOOLEAN	PIXIT G4	Can the IUT send an END−PDU on request at state 5?
ST10_END	BOOLEAN	PIXIT G5	Can the IUT send an END−PDU on request at state 10?
ST10_RS	BOOLEAN	PIXIT G6	Can the IUT send a RS−PDU on request at state 10?
ST10_POLL	BOOLEAN	PIXIT G7	Can the IUT send a POLL−PDU on request at state 10?
ST10_SD	BOOLEAN	PIXIT G8	Can the IUT send a SD−PDU on request at state 10?
Detailed Comments			

Test Case Selection Expression Definitions		
Expression Name	Selection Expression	Comments
State1_BGN	ST1_BGN	Can the IUT send a BGN−PDU on request at state 1?
State4_BGN	ST4_BGN	Can the IUT send a BGN−PDU on request at state 4?
State2_END	ST2_END	Can the IUT send an END−PDU on request at state 2?
State5_END	ST5_END	Can the IUT send an END−PDU on request at state 5?
State10_END	ST10_END	Can the IUT send an END−PDU on request at state 10?
State10_RS	ST10_RS	Can the IUT send a RS−PDU on request at state 10?
State10_POLL	ST10_POLL	Can the IUT send a POLL−PDU on request at state 10?
State10_SD	ST10_SD	Can the IUT send a SD−PDU on request at state 10?
State10_S_P	ST10_SD OR ST10_POLL	Can the IUT send a SD−PDU and a POLL−PDU on request at state 10?
Detailed Comments		

Test Suite Variable Declarations			
Variable Name	Type	Value	Comments
VT_SQ	INTEGER	0	Transmitter Connection Sequence state variable
VR_SQ	INTEGER	0	Receiver Connection Sequence state variable
Detailed Comments			

Test Case Variable Declarations			
Variable Name	Type	Value	Comments
VT_MS	INTEGER	0	Maximum Send state variable
VR_MR	INTEGER		Maximum Receive state variable
VT_S	INTEGER	0	Send state variable
VT_PS	INTEGER	0	Poll Send state variable
VT_A	INTEGER	0	Acknowledge state variable
VT_PA	INTEGER	0	Poll Acknowledge state variable
VT_PD	INTEGER	0	Poll Data state variable
VR_R	INTEGER	0	Receive state variable
VR_H	INTEGER	0	Highest expected state variable
count	INTEGER	0	general purpose counter
TCV_OCT	HEXSTRING		general purpose
TCV_N_SQ	INTEGER	0	to handle N(SQ)
TCV_N_MR	INTEGER	0	to handle N(MR)
TCV_N_PS	INTEGER	0	to handle N(PS)
TCV_LIST	LIST_TYPE	{}	to handle LIST field of STAT PDU
TCV_LIST1	LIST_TYPE	{}	to handle LIST field of STAT PDU
Detailed Comments			

PCO Type Declarations		
PCO Type	Role	Comments
L_SSCOP	LT	
Detailed Comments		

PCO Declarations			
PCO Name	PCO Type	Role	Comments
LT_PCO	L_SSCOP	LT	Lower boundary of SSCOP
Detailed Comments			

Timer Declarations			
Timer Name	Duration	Unit	Comments
T_Opr	TESTtime	s	This timer is used to allow test operator intervention
Timer_CC	TimerCCtime	ms	The time between transmission of BGN, END, ER, or RS PDU
Timer_POLL	TimerPOLLtime	ms	The time between transmission of POLL PDU at active phase
Timer_KEEP_ALIVE	TimerKEEP_ALIVEtime	s	The time between transmission of POLL PDU at transient phase
Timer_IDLE	TimerIDLEtime	s	may be considerably greater than Timer_KEEP_ALIVE
Timer_NO_RESPONSE	TimerNO_RESPONSEtime	s	The maximum time interval during which at least one STAT PDU needs to be received.
T_Wait	WAITtime	ms	This timer is used when no response is expected from IUT
Detailed Comments			

PDU Type Definition

PDU Name : BGAK
PCO Type : L_SSCOP
Encoding Rule Name :
Encoding Variation :
Comments :

Field Name	Field Type	Field Encoding	Comments
UU	OCTETSTRING[0..UU_Max_Len]		
PAD	OCTETSTRING[0..3]		
RESERVED	OCTETSTRING[4]		
PL	BITSTRING[2]		
RSVD	BITSTRING[2]		
PDU_Type	BITSTRING[4]		
N_MR	BITSTRING[24]		

Detailed Comments :

PDU Type Definition

PDU Name : BGN
PCO Type : L_SSCOP
Encoding Rule Name :
Encoding Variation :
Comments :

Field Name	Field Type	Field Encoding	Comments
UU	OCTETSTRING[0..UU_Max_Len]		
PAD	OCTETSTRING[0..3]		
RESERVED	OCTETSTRING[3]		
N_SQ	BITSTRING[8]		
PL	BITSTRING[2]		
RSVD	BITSTRING[2]		
PDU_Type	BITSTRING[4]		
N_MR	BITSTRING[24]		

Detailed Comments :

PDU Type Definition			
PDU Name : BGREJ			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Type	Field Encoding	Comments
UU	OCTETSTRING[0..UU_Max_Len]		
PAD	OCTETSTRING[0..3]		
RESERVED1	OCTETSTRING[4]		
PL	BITSTRING[2]		
RSVD	BITSTRING[2]		
PDU_Type	BITSTRING[4]		
RESERVED2	OCTETSTRING[3]		
Detailed Comments			

PDU Type Definition			
PDU Name : ENDAK			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Type	Field Encoding	Comments
RESERVED1	OCTETSTRING[4]		
RESERVED2	BITSTRING[4]		
PDU_Type	BITSTRING[4]		
RESERVED3	OCTETSTRING[3]		
Detailed Comments			

PDU Type Definition			
PDU Name : ENDPDU			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Type	Field Encoding	Comments
UU	OCTETSTRING[0..UU_Max_Len]		
PAD	OCTETSTRING[0..3]		
RESERVED1	OCTETSTRING[4]		
PL	BITSTRING[2]		
RR	BITSTRING[1]		"R" is a reserved word in TTCN.
S	BITSTRING[1]		
PDU_Type	BITSTRING[4]		
RESERVED2	OCTETSTRING[3]		
Detailed Comments			

PDU Type Definition			
PDU Name : ER			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Type	Field Encoding	Comments
RESERVED	OCTETSTRING[3]		
N_SQ	BITSTRING[8]		
RSVD	BITSTRING[4]		
PDU_Type	BITSTRING[4]		
N_MR	BITSTRING[24]		
Detailed Comments			

PDU Type Definition			
PDU Name : ERAK			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Type	Field Encoding	Comments
RESERVED	OCTETSTRING[4]		
RSVD	BITSTRING[4]		
PDU_Type	BITSTRING[4]		
N_MR	BITSTRING[24]		
Detailed Comments			

PDU Type Definition			
PDU Name : IVBGAK			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a BGAK PDU of incorrect length			
Field Name	Field Type	Field Encoding	Comments
UUandPAD	HEXSTRING[0..INFINITY]		to generate a PDU of incorrect length
RESERVED	OCTETSTRING[4]		
PL	BITSTRING[2]		
RSVD	BITSTRING[2]		
PDU_Type	BITSTRING[4]		
N_MR	BITSTRING[24]		
Detailed Comments			

PDU Type Definition			
PDU Name : IVBGN			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a BGN PDU of incorrect length			
Field Name	Field Type	Field Encoding	Comments
UUandPAD	HEXSTRING[0..INFINITY]		to generate a PDU of incorrect length
RESERVED	OCTETSTRING[3]		
N_SQ	BITSTRING[8]		
PL	BITSTRING[2]		
RSVD	BITSTRING[2]		
PDU_Type	BITSTRING[4]		
N_MR	BITSTRING[24]		
Detailed Comments: PAD field can be 6 octets(normally 3 octets).			

PDU Type Definition			
PDU Name : IVBGREJ			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a BGREJ PDU of incorrect length			
Field Name	Field Type	Field Encoding	Comments
UUandPAD	HEXSTRING[0..INFINITY]		to generate a PDU of incorrect length
RESERVED1	OCTETSTRING[4]		
PL	BITSTRING[2]		
RSVD	BITSTRING[2]		
PDU_Type	BITSTRING[4]		
RESERVED2	OCTETSTRING[3]		
Detailed Comments			

PDU Type Definition			
PDU Name : IVEND			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a END PDU of incorrec length			
Field Name	Field Type	Field Encoding	Comments
UUandPAD	HEXSTRING[0..INFINITY]		to generate a PDU of incorrect length
RESERVED1	OCTETSTRING[4]		
PL	BITSTRING[2]		
RR	BITSTRING[1]		"R" is a reserved word in TTCN.
S	BITSTRING[1]		
PDU_Type	BITSTRING[4]		
RESERVED2	OCTETSTRING[3]		
Detailed Comments			

PDU Type Definition			
PDU Name : IVENDAK			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a ENDAK PDU of incorrect length			
Field Name	Field Type	Field Encoding	Comments
INVALID	OCTETSTRING[0..4]		
RESERVED1	OCTETSTRING[4]		
RESERVED2	BITSTRING[4]		
PDU_Type	BITSTRING[4]		
RESERVED3	OCTETSTRING[3]		
Detailed Comments			

PDU Type Definition			
PDU Name : IVER			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a ER PDU of incorrect length			
Field Name	Field Type	Field Encoding	Comments
INVALID	OCTETSTRING[0..4]		
RESERVED	OCTETSTRING[3]		
N_SQ	BITSTRING[8]		
RSVD	BITSTRING[4]		
PDU_Type	BITSTRING[4]		
N_MR	BITSTRING[24]		
Detailed Comments :			

PDU Type Definition			
PDU Name : IVERAK			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a ERAK PDU of incorrect length			
Field Name	Field Type	Field Encoding	Comments
INVALID	OCTETSTRING[0..4]		
RESERVED	OCTETSTRING[4]		
RSVD	BITSTRING[4]		
PDU_Type	BITSTRING[4]		
N_MR	BITSTRING[24]		
Detailed Comments :			

PDU Type Definition			
PDU Name : IVMD			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a MD PDU of incorrect langth			
Field Name	Field Type	Field Encoding	Comments
InformationandPAD	HEXSTRING[0..INFINITY]		to generate a PDU of incorrect length
PL	BITSTRING[2]		
RSVD	BITSTRING[2]		
PDU_Type	BITSTRING[4]		
RESERVED	OCTETSTRING[3]		
Detailed Comments :			

PDU Type Definition			
PDU Name : IVPOLL			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a POLL PDU of incorrect length			
Field Name	Field Type	Field Encoding	Comments
INVALID	OCTETSTRING[0..4]		
RESERVED1	OCTETSTRING[1]		
N_PS	BITSTRING[24]		
RESERVED2	BITSTRING[4]		
PDU_Type	BITSTRING[4]		
N_S	BITSTRING[24]		
Detailed Comments			

PDU Type Definition			
PDU Name : IVRS			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a RS PDU of incorrect length			
Field Name	Field Type	Field Encoding	Comments
UUandPAD	HEXSTRING[0..INFINITY]		to generate a PDU of incorrect length
RESERVED	OCTETSTRING[3]		
N_SQ	BITSTRING[8]		
PL	BITSTRING[2]		
RSVD	BITSTRING[2]		
PDU_Type	BITSTRING[4]		
N_MR	BITSTRING[24]		
Detailed Comments :			

PDU Type Definition			
PDU Name : IVRSAK			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a RSAK PDU of incorrect length			
Field Name	Field Type	Field Encoding	Comments
INVALID	OCTETSTRING[0..4]		
RESERVED1	OCTETSTRING[4]		
RESERVED2	BITSTRING[4]		
PDU_Type	BITSTRING[4]		
N_MR	BITSTRING[24]		
Detailed Comments :			

PDU Type Definition			
PDU Name : IVSD			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a SD PDU of incorrect length			
Field Name	Field Type	Field Encoding	Comments
InformationandPAD	HEXSTRING[0..INFINITY]		to generate a PDU of incorrect length
PL	BITSTRING[2]		
RSVD	BITSTRING[2]		
PDU_Type	BITSTRING[4]		
N_S	BITSTRING[24]		
Detailed Comments :			

PDU Type Definition			
PDU Name : IVSTAT			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a STAT PDU whcih is not 32−bit aligned			
Field Name	Field Type	Field Encoding	Comments
INVALID	OCTETSTRING[0..4]		
LIST	HEXSTRING[0..INFINITY]		
RSVD1	OCTETSTRING[1]		
N_PS	BITSTRING[24]		
RSVD2	OCTETSTRING[1]		
N_MR	BITSTRING[24]		
RESERVED	BITSTRING[4]		
PDU_Type	BITSTRING[4]		
N_R	BITSTRING[24]		
Detailed Comments :			

PDU Type Definition			
PDU Name : IVUD			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a UD PDU of incorrect langth			
Field Name	Field Type	Field Encoding	Comments
InformationandPAD	HEXSTRING[0..INFINITY]		to generate a PDU of incorrect length
PL	BITSTRING[2]		
RSVD	BITSTRING[2]		
PDU_Type	BITSTRING[4]		
RESERVED	OCTETSTRING[3]		
Detailed Comments :			

PDU Type Definition			
PDU Name : IVUSTAT			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a USTAT PDU of incorrect length			
Field Name	Field Type	Field Encoding	Comments
INVALID	OCTETSTRING[0..4]		
PAD1	OCTETSTRING[1]		
LE1	BITSTRING[24]		
PAD2	OCTETSTRING[1]		
LE2	BITSTRING[24]		
RESERVED1	OCTETSTRING[1]		
N_MR	BITSTRING[24]		
RESERVED2	BITSTRING[4]		
PDU_Type	BITSTRING[4]		
N_R	BITSTRING[24]		
Detailed Comments :			

PDU Type Definition			
PDU Name : MD			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Type	Field Encoding	Comments
Information	OCTETSTRING[0..Info_Max_Len]		
PAD	OCTETSTRING[0..3]		
PL	BITSTRING[2]		
RSVD	BITSTRING[2]		
PDU_Type	BITSTRING[4]		
RESERVED	OCTETSTRING[3]		
Detailed Comments :			

PDU Type Definition			
PDU Name : POLL			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Type	Field Encoding	Comments
RESERVED1	OCTETSTRING[1]		
N_PS	BITSTRING[24]		
RESERVED2	BITSTRING[4]		
PDU_Type	BITSTRING[4]		
N_S	BITSTRING[24]		
Detailed Comments :			

PDU Type Definition			
PDU Name : RS			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Type	Field Encoding	Comments
UU	OCTETSTRING[0..UU_Max_Len]		
PAD	OCTETSTRING[0..3]		
RESERVED	OCTETSTRING[3]		
N_SQ	BITSTRING[8]		
PL	BITSTRING[2]		
RSVD	BITSTRING[2]		
PDU_Type	BITSTRING[4]		
N_MR	BITSTRING[24]		
Detailed Comments			

PDU Type Definition			
PDU Name : RSAK			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Type	Field Encoding	Comments
RESERVED1	OCTETSTRING[4]		
RESERVED2	BITSTRING[4]		
PDU_Type	BITSTRING[4]		
N_MR	BITSTRING[24]		
Detailed Comments			

PDU Type Definition			
PDU Name : SD			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Type	Field Encoding	Comments
Information	OCTETSTRING[0..Info_Max_Len]		
PAD	OCTETSTRING[0..3]		
PL	BITSTRING[2]		
RSVD	BITSTRING[2]		
PDU_Type	BITSTRING[4]		
N_S	BITSTRING[24]		
Detailed Comments :			

PDU Type Definition			
PDU Name : STAT			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Type	Field Encoding	Comments
LIST	LIST_TYPE		
RSVD1	OCTETSTRING[1]		
N_PS	BITSTRING[24]		
RSVD2	OCTETSTRING[1]		
N_MR	BITSTRING[24]		
RESERVED	BITSTRING[4]		
PDU_Type	BITSTRING[4]		
N_R	BITSTRING[24]		
Detailed Comments :			

PDU Type Definition			
PDU Name : UD			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Type	Field Encoding	Comments
Information	OCTETSTRING[0..Info_Max_Len]		
PAD	OCTETSTRING[0..3]		
PL	BITSTRING[2]		
RSVD	BITSTRING[2]		
PDU_Type	BITSTRING[4]		
RESERVED	OCTETSTRING[3]		
Detailed Comments :			

PDU Type Definition			
PDU Name : USTAT			
PCO Type : L_SSCOP			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Type	Field Encoding	Comments
PAD1	OCTETSTRING[1]		
LE1	BITSTRING[24]		
PAD2	OCTETSTRING[1]		
LE2	BITSTRING[24]		
RESERVED1	OCTETSTRING[1]		
N_MR	BITSTRING[24]		
RESERVED2	BITSTRING[4]		
PDU_Type	BITSTRING[4]		
N_R	BITSTRING[24]		
Detailed Comments :			

III

Constraints Part

PDU Constraint Declaration

Constraint Name : BGAK_R_GEN
PDU Type : BGAK
Derivation Path :
Encoding Rule Name :
Encoding Variation :
Comments : General RECEIVE constraint

Field Name	Field Value	Field Encoding	Comments
UU	*		
PAD	*		
RESERVED	'00000000'O		
PL	?		
RSVD	'00'B		
PDU_Type	'0010'B		
N_MR	?		

Detailed Comments

PDU Constraint Declaration

Constraint Name : BGAK_S_GEN(parN_MR:INTEGER)
PDU Type : BGAK
Derivation Path :
Encoding Rule Name :
Encoding Variation :
Comments :

Field Name	Field Value	Field Encoding	Comments
UU	-		
PAD	-		
RESERVED	'00000000'O		
PL	'00'B		
RSVD	'00'B		
PDU_Type	'0010'B		
N_MR	INT_TO_BIT(parN_MR,24)		

Detailed Comments

PDU Constraint Declaration			
Constraint Name : BGAK_S_INV(parN_MR:INTEGER)			
PDU Type : BGAK			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : an invalid BGAK PDU which is not 32−bit aligned			
Field Name	Field Value	Field Encoding	Comments
UU	'00000000000000000000'O		10 octets, PAD must be 2 octets
PAD	'000000'O		3 octets
RESERVED	'00000000'O		
PL	'00'B		
RSVD	'00'B		
PDU_Type	'0010'B		
N_MR	INT_TO_BIT(parN_MR,24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : BGN_R_GEN(parN_SQ:INTEGER)			
PDU Type : BGN			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : General RECEIVE constraint			
Field Name	Field Value	Field Encoding	Comments
UU	*		
PAD	*		
RESERVED	'000000'O		
N_SQ	COMPLEMENT(INT_TO_BIT (parN_SQ,8))		retransmitted BGN PDU check
PL	?		
RSVD	'00'B		
PDU_Type	'0001'B		
N_MR	?		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : BGN_R_RET(parN_SQ,parN_MR:INTEGER)			
PDU Type : BGN			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : constraint for retransmitted BGN PDU			
Field Name	Field Value	Field Encoding	Comments
UU	*		
PAD	*		
RESERVED	'000000'O		
N_SQ	INT_TO_BIT(parN_SQ,8)		
PL	?		
RSVD	'00'B		
PDU_Type	'0001'B		
N_MR	INT_TO_BIT(parN_MR,24)		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : BGN_S_CODE(parN_SQ,parN_MR:INTEGER)			
PDU Type : BGN			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : an invalid PDU which has an unknown PDU type code			
Field Name	Field Value	Field Encoding	Comments
UU	–		
PAD	–		
RESERVED	'000000'O		
N_SQ	INT_TO_BIT(parN_SQ,8)		
PL	'00'B		
RSVD	'00'B		
PDU_Type	'0000'B		
N_MR	INT_TO_BIT(parN_MR,24)		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : BGN_S_GEN(parN_SQ,parN_MR:INTEGER)			
PDU Type : BGN			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Value	Field Encoding	Comments
UU	–		
PAD	–		
RESERVED	'000000'O		
N_SQ	INT_TO_BIT(parN_SQ,8)		
PL	'00'B		
RSVD	'00'B		
PDU_Type	'0001'B		
N_MR	INT_TO_BIT(parN_MR,24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : BGN_S_INV(parN_SQ,parN_MR:INTEGER)			
PDU Type : BGN			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : an invalid BGN PDU which is not 32−bit aligned			
Field Name	Field Value	Field Encoding	Comments
UU	'00000000000000000000'O		10 octets, PAD must be 2 octets
PAD	'000000'O		3 octets
RESERVED	'000000'O		
N_SQ	INT_TO_BIT(parN_SQ,8)		
PL	'00'B		
RSVD	'00'B		
PDU_Type	'0001'B		
N_MR	INT_TO_BIT(parN_MR,24)		
Detailed Comments :			

PDU Constraint Declaration

Constraint Name : BGREJ_R_GEN
PDU Type : BGREJ
Derivation Path :
Encoding Rule Name :
Encoding Variation :
Comments : General RECEIVE constraint

Field Name	Field Value	Field Encoding	Comments
UU	*		
PAD	*		
RESERVED1	'00000000'O		
PL	?		
RSVD	'00'B		
PDU_Type	'0111'B		
RESERVED2	'000000'O		

Detailed Comments

PDU Constraint Declaration

Constraint Name : BGREJ_S_GEN
PDU Type : BGREJ
Derivation Path :
Encoding Rule Name :
Encoding Variation :
Comments :

Field Name	Field Value	Field Encoding	Comments
UU	–		
PAD	–		
RESERVED1	'00000000'O		
PL	'00'B		
RSVD	'00'B		
PDU_Type	'0111'B		
RESERVED2	'000000'O		

Detailed Comments

PDU Constraint Declaration			
Constraint Name : BGREJ_S_INV			
PDU Type : BGREJ			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : an invali BGREJ PDU which is not 32−bit aligned			
Field Name	Field Value	Field Encoding	Comments
UU	'00000000000000000000'O		10 octets, PAD must be 2 octets
PAD	'000000'O		3 octets
RESERVED1	'00000000'O		
PL	'00'B		
RSVD	'00'B		
PDU_Type	'0111'B		
RESERVED2	'000000'O		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : ENDAK_R_GEN			
PDU Type : ENDAK			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : General RECEIVE constraint			
Field Name	Field Value	Field Encoding	Comments
RESERVED1	'00000000'O		
RESERVED2	'0000'B		
PDU_Type	'0100'B		
RESERVED3	'000000'O		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : ENDAK_S_GEN			
PDU Type : ENDAK			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Constraint for normal SEND			
Field Name	Field Value	Field Encoding	Comments
RESERVED1	'00000000'O		
RESERVED2	'0000'B		
PDU_Type	'0100'B		
RESERVED3	'000000'O		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : END_R_GEN			
PDU Type : ENDPDU			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : general RECEIVE constraint			
Field Name	Field Value	Field Encoding	Comments
UU	*		
PAD	*		
RESERVED1	'00000000'O		
PL	?		
RR	'0'B		
S	?		IUT resend the last END PDU sent
PDU_Type	'0011'B		
RESERVED2	'000000'O		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : END_R_SSCOP			
PDU Type : ENDPDU			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : RECEIVE constraint for SSCOP initiated release			
Field Name	Field Value	Field Encoding	Comments
UU	–		
PAD	–		
RESERVED1	'00000000'O		
PL	'00'B		
RR	'0'B		
S	'1'B		SSCOP initiated release
PDU_Type	'0011'B		
RESERVED2	'000000'O		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : END_R_USER			
PDU Type : ENDPDU			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : RECEIVE constraint for USER initiated release			
Field Name	Field Value	Field Encoding	Comments
UU	*		
PAD	*		
RESERVED1	'00000000'O		
PL	?		
RR	'0'B		
S	'0'B		user initiated release
PDU_Type	'0011'B		
RESERVED2	'000000'O		
Detailed Comments			

PDU Constraint Declaration

Constraint Name : END_S_INV
PDU Type : ENDPDU
Derivation Path :
Encoding Rule Name :
Encoding Variation :
Comments : an invalid END PDU which is not 32−bit aligned

Field Name	Field Value	Field Encoding	Comments
UU	'00000000000000000000'O		10 octets, PAD must be 2 octets
PAD	'000000'O		3 octets
RESERVED1	'00000000'O		
PL	'00'B		
RR	'0'B		
S	'0'B		
PDU_Type	'0011'B		
RESERVED2	'000000'O		

Detailed Comments :

PDU Constraint Declaration

Constraint Name : END_S_SSCOP
PDU Type : ENDPDU
Derivation Path :
Encoding Rule Name :
Encoding Variation :
Comments : SEND constraint for SSCOP initiated release

Field Name	Field Value	Field Encoding	Comments
UU	−		
PAD	−		
RESERVED1	'00000000'O		
PL	'00'B		
RR	'0'B		
S	'1'B		
PDU_Type	'0011'B		
RESERVED2	'000000'O		

Detailed Comments :

PDU Constraint Declaration

Constraint Name : END_S_USER
PDU Type : ENDPDU
Derivation Path :
Encoding Rule Name :
Encoding Variation :
Comments : SEND constraint for USER initiated release

Field Name	Field Value	Field Encoding	Comments
UU	–		
PAD	–		
RESERVED1	'00000000'O		
PL	'00'B		
RR	'0'B		
S	'0'B		
PDU_Type	'0011'B		
RESERVED2	'000000'O		

Detailed Comments

PDU Constraint Declaration

Constraint Name : ERAK_R_GEN
PDU Type : ERAK
Derivation Path :
Encoding Rule Name :
Encoding Variation :
Comments : General RECEIVE constraint

Field Name	Field Value	Field Encoding	Comments
RESERVED	'00000000'O		
RSVD	'0000'B		
PDU_Type	'1111'B		
N_MR	?		

Detailed Comments

PDU Constraint Declaration			
Constraint Name : ERAK_S_GEN(parN_MR:INTEGER)			
PDU Type : ERAK			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Constraint for normal SEND			
Field Name	Field Value	Field Encoding	Comments
RESERVED	'00000000'O		
RSVD	'0000'B		
PDU_Type	'1111'B		
N_MR	INT_TO_BIT(parN_MR, 24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : ER_R_GEN(parN_SQ:INTEGER)			
PDU Type : ER			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : General RECEIVE constraint			
Field Name	Field Value	Field Encoding	Comments
RESERVED	'000000'O		
N_SQ	COMPLEMENT(INT_TO_BIT (parN_SQ,8))		retransmitted ER PDU check
RSVD	'0000'B		
PDU_Type	'1001'B		
N_MR	?		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : ER_R_RET(parN_SQ,parN_MR:INTEGER)			
PDU Type : ER			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : constraint for retransmitted RS PDU			
Field Name	Field Value	Field Encoding	Comments
RESERVED	'000000'O		
N_SQ	INT_TO_BIT(parN_SQ,8)		
RSVD	'0000'B		
PDU_Type	'1001'B		
N_MR	INT_TO_BIT(parN_MR,24)		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : ER_S_GEN(parN_SQ,parN_MR:INTEGER)			
PDU Type : ER			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Constraint fro normal SEND			
Field Name	Field Value	Field Encoding	Comments
RESERVED	'000000'O		
N_SQ	INT_TO_BIT(parN_SQ,8)		
RSVD	'0000'B		
PDU_Type	'1001'B		
N_MR	INT_TO_BIT(parN_MR,24)		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : IVBGAK_S_INV(parUUandPAD:HEXSTRING;parN_MR:INTEGER)			
PDU Type : IVBGAK			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a BGN PDU of incorrect length			
Field Name	Field Value	Field Encoding	Comments
UUandPAD	parUUandPAD		to generate a PDU of incorrect length
RESERVED	'00000000'O		
PL	'00'B		
RSVD	'00'B		
PDU_Type	'0010'B		
N_MR	INT_TO_BIT(parN_MR,24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : IVBGN_S_INV(parUUandPAD:HEXSTRING;parN_SQ,parN_MR:INTEGER)			
PDU Type : IVBGN			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a BGN PDU of incorrect length			
Field Name	Field Value	Field Encoding	Comments
UUandPAD	parUUandPAD		to generate a PDU of incorrect length
RESERVED	'000000'O		
N_SQ	INT_TO_BIT(parN_SQ,8)		
PL	'00'B		
RSVD	'00'B		
PDU_Type	'0001'B		
N_MR	INT_TO_BIT(parN_MR,24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : IVBGREJ_S_INV(parUUandPAD:HEXSTRING)			
PDU Type : IVBGREJ			
Derivation Path :			
Encoding Rule Name:			
Encoding Variation:			
Comments : Used to generate a BGREJ PDU of incorrect length			
Field Name	Field Value	Field Encoding	Comments
UUandPAD	parUUandPAD		to generate a PDU of incorrect length
RESERVED1	'00000000'O		
PL	'00'B		
RSVD	'00'B		
PDU_Type	'0111'B		
RESERVED2	'000000'O		
Detailed Comments:			

PDU Constraint Declaration			
Constraint Name : IVENDAK_S_INV(parINVALID:OCTETSTRING)			
PDU Type : IVENDAK			
Derivation Path :			
Encoding Rule Name:			
Encoding Variation:			
Comments : an ENDAK PDU of incorrect length			
Field Name	Field Value	Field Encoding	Comments
INVALID	parINVALID		
RESERVED1	'00000000'O		
RESERVED2	'0000'B		
PDU_Type	'0100'B		
RESERVED3	'000000'O		
Detailed Comments:			

PDU Constraint Declaration			
Constraint Name : IVEND_S_INV(parUUandPAD:HEXSTRING)			
PDU Type : IVEND			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a END PDU of incorrect length			
Field Name	Field Value	Field Encoding	Comments
UUandPAD	parUUandPAD		to generate a PDU of incorrect length
RESERVED1	'00000000'O		
PL	'00'B		
RR	'0'B		
S	'0'B		
PDU_Type	'0011'B		
RESERVED2	'000000'O		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : IVERAK_S_INV(parINVALID:OCTETSTRING;parN_MR:INTEGER)			
PDU Type : IVERAK			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : an ERAK PDU of incorrect length			
Field Name	Field Value	Field Encoding	Comments
INVALID	parINVALID		
RESERVED	'00000000'O		
RSVD	'0000'B		
PDU_Type	'1111'B		
N_MR	INT_TO_BIT(parN_MR, 24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : IVER_S_INV(parINVALID:OCTETSTRING;parN_SQ,parN_MR:INTEGER)			
PDU Type : IVER			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : an ER PDU of incorrect length			
Field Name	Field Value	Field Encoding	Comments
INVALID	parINVALID		
RESERVED	'000000'O		
N_SQ	INT_TO_BIT(parN_SQ,8)		
RSVD	'0000'B		
PDU_Type	'1001'B		
N_MR	INT_TO_BIT(parN_MR,24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : IVMD_S_INV(parInformationandPAD:HEXSTRING)			
PDU Type : IVMD			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a MD PDU of incorrect length			
Field Name	Field Value	Field Encoding	Comments
InformationandPAD	parInformationandPAD		to generate a PDU of incorrect length
PL	'11'B		
RSVD	'00'B		
PDU_Type	'1110'B		
RESERVED	'000000'O		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : IVPOLL_S_INV(parINVALID:OCTETSTRING;parN_PS,parN_S:INTEGER)			
PDU Type : IVPOLL			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Constraint for SEND			
Field Name	Field Value	Field Encoding	Comments
INVALID	parINVALID		
RESERVED1	'00'O		
N_PS	INT_TO_BIT(parN_PS,24)		
RESERVED2	'0000'B		
PDU_Type	'1010'B		
N_S	INT_TO_BIT(parN_S,24)		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : IVRSAK_S_INV(parINVALID:OCTETSTRING;parN_MR:INTEGER)			
PDU Type : IVRSAK			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : an RSAK PDU of incorrect length			
Field Name	Field Value	Field Encoding	Comments
INVALID	parINVALID		
RESERVED1	'00000000'O		
RESERVED2	'0000'B		
PDU_Type	'0110'B		
N_MR	INT_TO_BIT(parN_MR, 24)		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : IVRS_S_INV(parUUandPAD:HEXSTRING;parN_SQ,parN_MR:INTEGER)			
PDU Type : IVRS			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a END PDU of incorrect length			
Field Name	Field Value	Field Encoding	Comments
UUandPAD	parUUandPAD		to generate a PDU of incorrect length
RESERVED	'000000'O		
N_SQ	INT_TO_BIT(parN_SQ,8)		
PL	'00'B		
RSVD	'00'B		
PDU_Type	'0101'B		
N_MR	INT_TO_BIT(parN_MR,24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : IVSD_S_INV(parInformationandPAD:HEXSTRING;parN_S:INTEGER)			
PDU Type : IVSD			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a SD PDU of incorrect length			
Field Name	Field Value	Field Encoding	Comments
InformationandPAD	parInformationandPAD		to generate a PDU of incorrect length
PL	'11'B		
RSVD	'00'B		
PDU_Type	'1000'B		
N_S	INT_TO_BIT(parN_S,24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : IVSTAT_S_INV(parLIST:HEXSTRING;parINVALID:OCTETSTRING;parN_PS,parN_MR,parN_R:INTEGER)			
PDU Type : IVSTAT			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : an STAT PDU which is not 32−bit aligned			
Field Name	Field Value	Field Encoding	Comments
INVALID	parINVALID		
LIST	parLIST		
RSVD1	'00'O		
N_PS	INT_TO_BIT(parN_PS,24)		
RSVD2	'00'O		
N_MR	INT_TO_BIT(parN_MR, 24)		
RESERVED	'0000'B		
PDU_Type	'1011'B		
N_R	INT_TO_BIT(parN_R, 24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : IVUD_S_INV(parInformationandPAD:HEXSTRING)			
PDU Type : IVUD			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Used to generate a UD PDU of incorrect length			
Field Name	Field Value	Field Encoding	Comments
InformationandPAD	parInformationandPAD		to generate a PDU of incorrect length
PL	'11'B		
RSVD	'00'B		
PDU_Type	'1101'B		
RESERVED	'000000'O		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : IVUSTAT_S_INV(parLE1,parLE2:INTEGER; parINVALID:OCTETSTRING;parN_MR,parN_R:INTEGER)			
PDU Type : IVUSTAT			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Constraint for SEND with elements variation.			
Field Name	Field Value	Field Encoding	Comments
INVALID	parINVALID		
PAD1	'00'O		
LE1	INT_TO_BIT(parLE1,24)		
PAD2	'00'O		
LE2	INT_TO_BIT(parLE2,24)		
RESERVED1	'00'O		
N_MR	INT_TO_BIT(parN_MR,24)		
RESERVED2	'0000'B		
PDU_Type	'1100'B		
N_R	INT_TO_BIT(parN_R, 24)		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : MD_R_GEN			
PDU Type : MD			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : General RECEIVE constraint			
Field Name	Field Value	Field Encoding	Comments
Information	*		
PAD	*		
PL	?		
RSVD	'00'B		
PDU_Type	'1110'B		
RESERVED	'000000'O		
Detailed Comments			

PDU Constraint Declaration

Constraint Name : MD_S_GEN
PDU Type : MD
Derivation Path :
Encoding Rule Name :
Encoding Variation :
Comments : Constraint for normal SEND

Field Name	Field Value	Field Encoding	Comments
Information	'0000000000'O		
PAD	'000000'O		
PL	'11'B		
RSVD	'00'B		
PDU_Type	'1110'B		
RESERVED	'000000'O		

Detailed Comments :

PDU Constraint Declaration

Constraint Name : MD_S_INV
PDU Type : MD
Derivation Path :
Encoding Rule Name :
Encoding Variation :
Comments : an invalid MD PDU which is not 32−bit aligned

Field Name	Field Value	Field Encoding	Comments
Information	'00000000000000000000'O		10 octets, PAD must be 2 octets
PAD	'000000'O		3 octets
PL	'11'B		
RSVD	'00'B		
PDU_Type	'1110'B		
RESERVED	'000000'O		

Detailed Comments :

PDU Constraint Declaration			
Constraint Name : POLL_R_GEN			
PDU Type : POLL			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : General RECEIVE constraint			
Field Name	Field Value	Field Encoding	Comments
RESERVED1	'00'O		
N_PS	?		
RESERVED2	'0000'B		
PDU_Type	'1010'B		
N_S	?		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : POLL_S_GEN(parN_PS,parN_S:INTEGER)			
PDU Type : POLL			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Constraint for SEND			
Field Name	Field Value	Field Encoding	Comments
RESERVED1	'00'O		
N_PS	INT_TO_BIT(parN_PS,24)		
RESERVED2	'0000'B		
PDU_Type	'1010'B		
N_S	INT_TO_BIT(parN_S,24)		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : POLL_S_N_S(parN_PS,parN_S:INTEGER)			
PDU Type : POLL			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Constraint for SEND with N_S variation			
Field Name	Field Value	Field Encoding	Comments
RESERVED1	'00'O		
N_PS	INT_TO_BIT(parN_PS,24)		
RESERVED2	'0000'B		
PDU_Type	'1010'B		
N_S	INT_TO_BIT(parN_S,24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : RSAK_R_GEN			
PDU Type : RSAK			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : General RECEIVE constraint			
Field Name	Field Value	Field Encoding	Comments
RESERVED1	'00000000'O		
RESERVED2	'0000'B		
PDU_Type	'0110'B		
N_MR	?		
Detailed Comments :			

PDU Constraint Declaration

Constraint Name : RSAK_S_GEN(parN_MR:INTEGER)
PDU Type : RSAK
Derivation Path :
Encoding Rule Name :
Encoding Variation :
Comments : Constraint for normal SEND

Field Name	Field Value	Field Encoding	Comments
RESERVED1	'00000000'O		
RESERVED2	'0000'B		
PDU_Type	'0110'B		
N_MR	INT_TO_BIT(parN_MR, 24)		

Detailed Comments :

PDU Constraint Declaration

Constraint Name : RS_R_GEN(parN_SQ:INTEGER)
PDU Type : RS
Derivation Path :
Encoding Rule Name :
Encoding Variation :
Comments : General RECEIVE constraint

Field Name	Field Value	Field Encoding	Comments
UU	*		
PAD	*		
RESERVED	'000000'O		
N_SQ	COMPLEMENT(INT_TO_BIT (parN_SQ,8))		retransmitted RS PDU check
PL	?		
RSVD	'00'B		
PDU_Type	'0101'B		
N_MR	?		

Detailed Comments :

PDU Constraint Declaration			
Constraint Name : RS_R_RET(parN_SQ,parN_MR:INTEGER)			
PDU Type : RS			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : constraint for retransmitted RS PDU			
Field Name	Field Value	Field Encoding	Comments
UU	*		
PAD	*		
RESERVED	'000000'O		
N_SQ	INT_TO_BIT(parN_SQ,8)		
PL	?		
RSVD	'00'B		
PDU_Type	'0101'B		
N_MR	INT_TO_BIT(parN_MR,24)		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : RS_S_GEN(parN_SQ,parN_MR:INTEGER)			
PDU Type : RS			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments :			
Field Name	Field Value	Field Encoding	Comments
UU	–		
PAD	–		
RESERVED	'000000'O		
N_SQ	INT_TO_BIT(parN_SQ,8)		
PL	'00'B		
RSVD	'00'B		
PDU_Type	'0101'B		
N_MR	INT_TO_BIT(parN_MR,24)		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : RS_S_INV(parN_SQ,parN_MR:INTEGER)			
PDU Type : RS			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : an invalid RS PDU which is not 32−bit aligned			
Field Name	Field Value	Field Encoding	Comments
UU	'00000000000000000000'O		10 octets, PAD must be 2 octets
PAD	'000000'O		3 octets
RESERVED	'000000'O		
N_SQ	INT_TO_BIT(parN_SQ,8)		
PL	'00'B		
RSVD	'00'B		
PDU_Type	'0101'B		
N_MR	INT_TO_BIT(parN_MR,24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : SD_R_GEN(parN_S:INTEGER)			
PDU Type : SD			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : General RECEIVE constraint			
Field Name	Field Value	Field Encoding	Comments
Information	*		
PAD	*		
PL	?		
RSVD	'00'B		
PDU_Type	'1000'B		
N_S	INT_TO_BIT(parN_S, 24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : SD_S_GEN(parN_S:INTEGER)			
PDU Type : SD			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Constraint for normal SEND			
Field Name	Field Value	Field Encoding	Comments
Information	'0000000000'O		Must be acceptable by IUT's upper layers
PAD	'000000'O		
PL	'11'B		
RSVD	'00'B		
PDU_Type	'1000'B		
N_S	INT_TO_BIT(parN_S,24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : SD_S_INV(parN_S:INTEGER)			
PDU Type : SD			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : an invalid SD PDU which is not 32−bit aligned			
Field Name	Field Value	Field Encoding	Comments
Information	'00000000000000000000'O		10 octets, PAD must be 2 octets
PAD	'000000'O		3 octets
PL	'11'B		
RSVD	'00'B		
PDU_Type	'1000'B		
N_S	INT_TO_BIT(parN_S,24)		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : SD_S_N_S(parN_S:INTEGER)			
PDU Type : SD			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Constraint for SEND with N_S variation			
Field Name	Field Value	Field Encoding	Comments
Information	'0000000000'O		
PAD	'000000'O		
PL	'11'B		
RSVD	'00'B		
PDU_Type	'1000'B		
N_S	INT_TO_BIT(parN_S,24)		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : STAT_R_LIST(parLIST:LIST_TYPE; parN_R:INTEGER)			
PDU Type : STAT			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Constraint for RECEIVE with elements			
Field Name	Field Value	Field Encoding	Comments
LIST	parLIST		
RSVD1	'00'O		
N_PS	?		
RSVD2	'00'O		
N_MR	?		
RESERVED	'0000'B		
PDU_Type	'1011'B		
N_R	INT_TO_BIT(parN_R, 24)		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : STAT_R_N_R(parN_R:INTEGER)			
PDU Type : STAT			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Constraint for RECEIVE without element			
Field Name	Field Value	Field Encoding	Comments
LIST	–		
RSVD1	'00'O		
N_PS	?		
RSVD2	'00'O		
N_MR	?		
RESERVED	'0000'B		
PDU_Type	'1011'B		
N_R	INT_TO_BIT(parN_R, 24)		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : STAT_R_N_R_S10_Verify(parN_PS:INTEGER)			
PDU Type : STAT			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Constraint for RECEIVE without element			
Field Name	Field Value	Field Encoding	Comments
LIST	*		
RSVD1	'00'O		
N_PS	INT_TO_BIT(parN_PS,24)		
RSVD2	'00'O		
N_MR	?		
RESERVED	'0000'B		
PDU_Type	'1011'B		
N_R	?		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : STAT_S_N_PS_N_R(parLIST:LIST_TYPE; parN_PS,parN_MR,parN_R:INTEGER)			
PDU Type : STAT			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Constraint for SEND with N_PS and N_R variations.			
Field Name	Field Value	Field Encoding	Comments
LIST	parLIST		
RSVD1	'00'O		
N_PS	INT_TO_BIT(parN_PS,24)		
RSVD2	'00'O		
N_MR	INT_TO_BIT(parN_MR, 24)		
RESERVED	'0000'B		
PDU_Type	'1011'B		
N_R	INT_TO_BIT(parN_R, 24)		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : UD_R_GEN			
PDU Type : UD			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : General RECEIVE constraint			
Field Name	Field Value	Field Encoding	Comments
Information	*		
PAD	*		
PL	?		
RSVD	'00'B		
PDU_Type	'1101'B		
RESERVED	'000000'O		
Detailed Comments			

PDU Constraint Declaration			
Constraint Name : UD_S_GEN			
PDU Type : UD			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : Constraint for normal SEND			
Field Name	Field Value	Field Encoding	Comments
Information	'0000000000'O		
PAD	'000000'O		
PL	'11'B		
RSVD	'00'B		
PDU_Type	'1101'B		
RESERVED	'000000'O		
Detailed Comments :			

PDU Constraint Declaration			
Constraint Name : UD_S_INV			
PDU Type : UD			
Derivation Path :			
Encoding Rule Name :			
Encoding Variation :			
Comments : an invalid UD PDU which is not 32−bit aligned			
Field Name	Field Value	Field Encoding	Comments
Information	'00000000000000000000'O		10 octets, PAD must be 2 octets
PAD	'000000'O		3 octets
PL	'11'B		
RSVD	'00'B		
PDU_Type	'1101'B		
RESERVED	'000000'O		
Detailed Comments :			

PDU Constraint Declaration

Constraint Name : USTAT_R_LIST(parLE1,parLE2:INTEGER; parN_R:INTEGER)
PDU Type : USTAT
Derivation Path :
Encoding Rule Name :
Encoding Variation :
Comments : Constraint for RECEIVE with LE variation

Field Name	Field Value	Field Encoding	Comments
PAD1	?		
LE1	INT_TO_BIT(parLE1, 24)		
PAD2	?		
LE2	INT_TO_BIT(parLE2, 24)		
RESERVED1	'00'O		
N_MR	?		
RESERVED2	'0000'B		
PDU_Type	'1100'B		
N_R	INT_TO_BIT(parN_R, 24)		

Detailed Comments :

PDU Constraint Declaration

Constraint Name : USTAT_S_LIST(parLE1,parLE2:INTEGER; parN_MR,parN_R:INTEGER)
PDU Type : USTAT
Derivation Path :
Encoding Rule Name :
Encoding Variation :
Comments : Constraint for SEND with elements variation.

Field Name	Field Value	Field Encoding	Comments
PAD1	'00'O		
LE1	INT_TO_BIT(parLE1,24)		
PAD2	'00'O		
LE2	INT_TO_BIT(parLE2,24)		
RESERVED1	'00'O		
N_MR	INT_TO_BIT(parN_MR,24)		
RESERVED2	'0000'B		
PDU_Type	'1100'B		
N_R	INT_TO_BIT(parN_R, 24)		

Detailed Comments :

IV

Dynamic Part

Test Case Dynamic Behaviour

Test Case Name: S1_V_A1

Group : PC/STATE_1/VAL/

Purpose : Verify that the IUT generates the BGN PDU on demand at state 1.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(5 of 51)/PICS PC11

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		<IUT!BGN>	BGN_R_GEN(VR_SQ)		
3		START T_Opr			
4	LB1	LT_PCO?BGN(VR_SQ:=BIT_TO_INT(BGN.N_SQ), VT_MS:=BIT_TO_INT(BGN.N_MR)) CANCEL T_Opr	BGN_R_GEN(VR_SQ)		
5		+S2_VERIFY			
6		+postamble			return the IUT in STATE 1
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Opr			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_V_P1

Group : PC/STATE_1/VAL/

Purpose : Verify that the IUT goes to state 3, if power−up robustness is implemented, or sends a BGREJ PDU, if not , on reception of retransmitted BGN PDU.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(5 of 51)/PICS PC12 and Ref X, Fig. 5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		N(SQ)=VR(SQ)
4		START Timer_CC			
5		[Power_up_robust]			
6	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR)) CANCEL Timer_CC	BGAK_R_GEN	(P)	assume a AA−ESTABLISH.response from SSCF UNI
7		+S10_VERIFY			
8		+postamble			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		+TS_CC			
14		[NOT(Power_up_robust)]			
15	LB2	LT_PCO?BGREJ CANCEL Timer_CC	BGREJ_R_GEN	(P)	
16		+S1_VERIFY			
17		+postamble			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB2			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB2			
22		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_V_P2

Group : PC/STATE_1/VAL/

Purpose : Verify that the IUT goes to state 3 on reception of BGN PDU at state 1.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(5 and 11 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		N(SQ)<>VR(SQ)
4		START Timer_CC			
5	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR)) CANCEL Timer_CC	BGAK_R_GEN	(P)	assume a AA−ESTABLISH.response from SSCF UNI
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?BGREJ CANCEL Timer_CC	BGREJ_R_GEN	(P)	(s1)
9		+S1_VERIFY			
10		+postamble			
11		LT_PCO?MD	MD_R_GEN		
12		GOTO LB1			
13		LT_PCO?UD	UD_R_GEN		
14		GOTO LB1			
15		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S1_V_P5					
Group : PC/STATE_1/VAL/					
Purpose : Verify that the IUT sends a ENDAK PDU on reception of a END PDU at state 1.					
Configuration :					
Default :					
Comments : Ref. 5.0 g, Fig. 20(5 of 51)/PICS PC8					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!ENDPDU	END_S_USER		
3		START Timer_CC			
4	LB1	LT_PCO?ENDAK CANCEL Timer_CC	ENDAK_R_GEN	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S1_V_P6
Group : PC/STATE_1/VAL/
Purpose : Verify that the IUT ignores a ENDAK PDU and remains at state 1.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(5 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!ENDAK	ENDAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_V_P16
Group : PC/STATE_1/VAL/
Purpose : Verify that the IUT accepts a UD PDU at state 1.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.2

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!UD	UD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_V_P17
Group : PC/STATE_1/VAL/
Purpose : Verify that the IUT accepts a MD PDU at state 1.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!MD	MD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:= GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_INV(VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments:

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I2

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGAK	BGAK_S_INV(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I3

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I4

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!ENDPDU	END_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I6

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!RS	RS_S_INV(VT_SQ,VR_MR)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I10

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!SD	SD_S_INV(VT_S)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I14
Group : PC/STATE_1/INV/
Purpose : Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 1.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!UD	UD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I15
Group : PC/STATE_1/INV/
Purpose : Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 1.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!MD	MD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I16

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR :=GET_VR_MR())			
4		LT_PCO!IVBGN	IVBGN_S_INV(TCV_OCT,VT_SQ,VR_MR)		
5		START T_Wait			
6	LB1	?TIMEOUT T_Wait		(P)	
7		+S1_VERIFY			
8		+postamble			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I17

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		(VR_MR:=GET_VR_MR())			
4		LT_PCO!IVBGAK	IVBGAK_S_INV(TCV_OCT, VR_MR)		
5		START T_Wait			
6	LB1	?TIMEOUT T_Wait		(P)	
7		+S1_VERIFY			
8		+postamble			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I18

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGREJ	IVBGREJ_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I19

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVEND	IVEND_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I20_1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('00000000'O)		extra 4 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I20_2

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('0000'O)		extra 2 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I21

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVRS	IVRS_S_INV(TCV_OCT,VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I22_1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('00000000' O,VR_MR)		extra 4 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I22_2

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('0000'O,VR_MR)		extra 2 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I23_1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('00000000'O,VT_SQ,VR_MR)		extra 4 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I23_2

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('0000'O,VT_SQ,VR_MR)		extra 2 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I24_1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('00000000' O,VR_MR)		extra 4 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I24_2

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('0000'O,VR_MR)		extra 2 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I25

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSD	IVSD_S_INV(TCV_OCT,VT_S)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I26_1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('00000000' O,VT_PS,VT_S)		extra 4 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I26_2

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('0000'O,VT_PS,VT_S)		extra 2 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I27_1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5,, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_OCT,'00000000'O,VT_PS,VR_MR, VR_R)		extra 4 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I27_2

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5,, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_OCT,'0000'O,VT_PS,VR_MR,VR_R)		extra 2 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I28_1

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'00000000'O,VR_MR,VR_R)		extra 4 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I28_2

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTST PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'0000'O,VR_MR,VR_R)		extra 2 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I29

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVUD	IVUD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I30

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVMD	IVMD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IV_I31

Group : PC/STATE_1/INV/

Purpose : Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 1.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_CODE(VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IO_P3

Group : PC/STATE_1/INOP/

Purpose : Verify that the IUT sends a END PDU on reception of a BGAK PDU at state 1.

Configuration :

Default :

Comments : Fig. 20(6 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGAK	BGAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	LT_PCO?ENDPDU CANCEL T_Wait	END_R_SSCOP	(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IO_P4

Group : PC/STATE_1/INOP/

Purpose : Verify that the IUT ignores a BGREJ PDU and remains at state 1.

Configuration :

Default :

Comments : Fig. 20(5 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IO_P8

Group : PC/STATE_1/INOP/

Purpose : Verify that the IUT sends a END PDU on reception of a RS PDU at state 1.

Configuration :

Default :

Comments : Fig. 20(7 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!RS	RS_S_GEN(VT_SQ,VR_MR)		
4		START Timer_CC			
5	LB1	LT_PCO?ENDPDU CANCEL Timer_CC	END_R_SSCOP	(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IO_P9

Group : PC/STATE_1/INOP/

Purpose : Verify that the IUT sends a END PDU on reception of a RSAK PDU at state 1.

Configuration :

Default :

Comments : Fig. 20(7 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!RSAK	RSAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	LT_PCO?ENDPDU CANCEL T_Wait	END_R_SSCOP	(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IO_P10

Group : PC/STATE_1/INOP/

Purpose : Verify that the IUT sends a END PDU on reception of a ER PDU at state 1.

Configuration :

Default :

Comments : Fig. 20(5 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!ER	ER_S_GEN(VT_SQ,VR_MR)		
4		START Timer_CC			
5	LB1	LT_PCO?ENDPDU CANCEL Timer_CC	END_R_SSCOP	(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IO_P11

Group : PC/STATE_1/INOP/

Purpose : Verify that the IUT sends a END PDU on reception of a ERAK PDU at state 1.

Configuration :

Default :

Comments : Fig. 20(6 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!ERAK	ERAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	LT_PCO?ENDPDU CANCEL T_Wait	END_R_SSCOP	(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IO_P12
Group : PC/STATE_1/INOP/
Purpose : Verify that the IUT sends a END PDU on reception of a SD PDU at state 1.
Configuration :
Default :
Comments : Fig. 20(6 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN(VT_S)		
3		START T_Wait			
4	LB1	LT_PCO?ENDPDU CANCEL T_Wait	END_R_SSCOP	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IO_P13
Group : PC/STATE_1/INOP/
Purpose : Verify that the IUT sends a END PDU on reception of a POLL PDU at state 1.
Configuration :
Default :
Comments : Fig. 20(6 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(VT_PS:=INC_MOD_24(VT_PS,1))			
3		LT_PCO!POLL	POLL_S_GEN(VT_PS,VT_S)		
4		START T_Wait			
5	LB1	LT_PCO?ENDPDU CANCEL T_Wait	END_R_SSCOP	(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IO_P14

Group : PC/STATE_1/INOP/

Purpose : Verify that the IUT sends a END PDU on reception of a STAT PDU at state 1.

Configuration :

Default :

Comments : Fig. 20(6 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!STAT	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_MR,VR_R)		list_length=0 no POLL PDU for TCV_N_PS
4		START T_Wait			
5	LB1	LT_PCO?ENDPDU CANCEL T_Wait	END_R_SSCOP	(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S1_IO_P15

Group : PC/STATE_1/INOP/

Purpose : Verify that the IUT sends a END PDU on reception of a USTAT PDU at state 1.

Configuration :

Default :

Comments : Fig. 20(6 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!USTAT	USTAT_S_LIST(1,3, VR_MR,1)		elements have no meaning
4		START T_Wait			
5	LB1	LT_PCO?ENDPDU CANCEL T_Wait	END_R_SSCOP	(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_A3

Group : PC/STATE_2/VAL/

Purpose : Verify that the IUT generates the END PDU on demand at state 2.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(9 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		<IUT!ENDPDU>	END_R_USER		
3		START T_Opr			
4	LB1	LT_PCO?ENDPDU CANCEL T_Opr	END_R_USER	(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
12		GOTO LB1			
13		+TS_Opr			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_P1

Group : PC/STATE_2/VAL/

Purpose : Verify that the IUT ignores a retransmitted BGN PDU at state 2

Configuration :

Default :

Comments : Fig. 20(10 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		N(SQ)=VR(SQ)
4		START Timer_CC			
5	LB1	?TIMEOUT Timer_CC		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_P2

Group : PC/STATE_2/VAL/

Purpose : Verify that the IUT sends a BGAK PDU on reception of BGN PDU and goes to state 10.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(10 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		N(SQ)<>VR(SQ)
4		START Timer_CC			
5	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR)) CANCEL Timer_CC	BGAK_R_GEN	(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_P3
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT goes to state 10 on reception of BGAK PDU at state 2.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGAK	BGAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?POLL	POLL_R_GEN		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_P4

Group : PC/STATE_2/VAL/

Purpose : Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 2.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_P5
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a END PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!ENDPDU	END_S_USER		
3		START Timer_CC			
4	LB1	?TIMEOUT Timer_CC		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_P6
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a ENDAK PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!ENDAK	ENDAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_P8

Group : PC/STATE_2/VAL/

Purpose : Verify that the IUT ignores a RS PDU and remains at state 2.

Configuration :

Default :

Comments : Fig. 20(10 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!RS	RS_S_GEN(VT_SQ,VR_MR)		
4		START Timer_CC			
5	LB1	?TIMEOUT Timer_CC		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_P9

Group : PC/STATE_2/VAL/

Purpose : Verify that the IUT ignores a RSAK PDU and remains at state 2.

Configuration :

Default :

Comments : Fig. 20(10 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!RSAK	RSAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_P10

Group : PC/STATE_2/VAL/

Purpose : Verify that the IUT ignores a ER PDU and remains at state 2.

Configuration :

Default :

Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!ER	ER_S_GEN(VT_SQ,VR_MR)		
4		START Timer_CC			
5	LB1	?TIMEOUT Timer_CC		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_P11
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a ERAK PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!ERAK	ERAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_P12
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a SD PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN(VT_S)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_P13
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a POLL PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(VT_PS:=INC_MOD_24(VT_PS,1))			
3		LT_PCO!POLL	POLL_S_GEN(VT_PS,VT_S)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S2_V_P14					
Group : PC/STATE_2/VAL/					
Purpose : Verify that the IUT ignores a STAT PDU and remains at state 2.					
Configuration :					
Default :					
Comments : Fig. 20(8 of 51)/PICS PC7					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!STAT	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_MR,VR_R)		list_length=0 no POLL PDU for TCV_N_PS
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S2_V_P15
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT ignores a USTAT PDU and remains at state 2.
Configuration :
Default :
Comments : Fig. 20(8 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!USTAT	USTAT_S_LIST(1,3,VR_MR, 1)		elements have no meaning
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_P16
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT accepts a UD PDU at state 2.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.2

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!UD	UD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_V_P17
Group : PC/STATE_2/VAL/
Purpose : Verify that the IUT accepts a MD PDU at state 2.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!MD	MD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S2_IV_I1					
Group : PC/STATE_2/INV/					
Purpose : Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 2.					
Configuration :					
Default :					
Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_INV(VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGAK	BGAK_S_INV(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I3

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I4

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!ENDPDU	END_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I6

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!RS	RS_S_INV(VT_SQ,VR_MR)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I10

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!SD	SD_S_INV(VT_S)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I14

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!UD	UD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I15

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!MD	MD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I16

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR :=GET_VR_MR())			
4		LT_PCO!IVBGN	IVBGN_S_INV(TCV_OCT,VT_SQ,VR_MR)		
5		START T_Wait			
6	LB1	?TIMEOUT T_Wait		(P)	
7		+S2_VERIFY			
8		+postamble			
9		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
10		GOTO LB1			
11		LT_PCO?MD	MD_R_GEN		
12		GOTO LB1			
13		LT_PCO?UD	UD_R_GEN		
14		GOTO LB1			
15		LT_PCO?OTHERWISE		(F)	
16		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I17

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		(VR_MR:=GET_VR_MR())			
4		LT_PCO!IVBGAK	IVBGAK_S_INV(TCV_OCT, VR_MR)		
5		START T_Wait			
6	LB1	?TIMEOUT T_Wait		(P)	
7		+S2_VERIFY			
8		+postamble			
9		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
10		GOTO LB1			
11		LT_PCO?MD	MD_R_GEN		
12		GOTO LB1			
13		LT_PCO?UD	UD_R_GEN		
14		GOTO LB1			
15		LT_PCO?OTHERWISE		(F)	
16		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I18

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGREJ	IVBGREJ_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I19

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVEND	IVEND_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I20_1

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('00000000'O)		extra 4 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I20_2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('0000'O)		extra 2 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S2_IV_I21					
Group : PC/STATE_2/INV/					
Purpose : Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 2.					
Configuration :					
Default :					
Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVRS	IVRS_S_INV(TCV_OCT,VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I22_1

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('00000000'O,VR_MR)		extra 4 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I22_2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('0000'O,VR_MR)		extra 2 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I23_1

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('00000000'O,VT_SQ,VR_MR)		extra 4 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I23_2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('0000'O,VT_SQ,VR_MR)		extra 2 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I24_1

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('00000000'O,VR_MR)		extra 4 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I24_2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('0000'O,VR_MR)		extra 2 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I25

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSD	IVSD_S_INV(TCV_OCT,VT_S)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I26_1

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('00000000'O,VT_PS,VT_S)		extra 4 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I26_2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('0000'O,VT_PS,VT_S)		extra 2 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I27_1

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_OCT,'00000000'O,VT_PS,VR_MR,VR_R)		extra 4 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I27_2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_OCT,'0000'O,VT_PS,VR_MR,VR_R)		extra 2 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I28_1

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'00000000'O,VR_MR,VR_R)		extra 4 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I28_2

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTST PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'0000'O,VR_MR,VR_R)		extra 2 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S2_IV_I29					
Group : PC/STATE_2/INV/					
Purpose : Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 2.					
Configuration :					
Default :					
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVUD	IVUD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S2_IV_I30

Group : PC/STATE_2/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 2.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVMD	IVMD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S2_IV_I31					
Group : PC/STATE_2/INV/					
Purpose : Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 2.					
Configuration :					
Default :					
Comments : Ref. 7.1, Fig. 20(47 of 51)/PICS PD3					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_CODE(VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S2_VERIFY			
7		+postamble			
8		LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S4_V_A1

Group : PC/STATE_4/VAL/

Purpose : Verify that the IUT generates the BGN PDU on demand at state 4.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(14 of 51)/PICS PC11

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		<IUT!BGN>	BGN_R_GEN(VR_SQ)		
3		START T_Opr			
4	LB1	LT_PCO?BGN(VR_SQ:=BIT_TO_INT(BGN.N_SQ), VT_MS:=BIT_TO_INT(BGN.N_MR)) CANCEL T_Opr	BGN_R_GEN(VR_SQ)		
5		+S2_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?ENDPDU	END_R_USER		
12		GOTO LB1			
13		+TS_Opr			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_V_P1

Group : PC/STATE_4/VAL/

Purpose : Verify that the IUT sends a BGAK and END PDU on reception of retransmitted BGN PDU at state 4.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(16 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		N(SQ)=VR(SQ)
4		START Timer_CC			
5	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR)) CANCEL Timer_CC	BGAK_R_GEN		
6		START T_Wait			
7	LB2	LT_PCO?ENDPDU CANCEL T_Wait	END_R_USER	(P)	resend the last END PDU sent
8		+S4_VERIFY			
9		+postamble			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB2			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB2			
14		+TS_Wait			
15		LT_PCO?MD	MD_R_GEN		
16		GOTO LB1			
17		LT_PCO?UD	UD_R_GEN		
18		GOTO LB1			
19		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_V_P2

Group : PC/STATE_4/VAL/

Purpose : Verify that the IUT goes to state 3 on reception of BGN PDU at state 4.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(16 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		N(SQ)<>VR(SQ) (s3)
4		START Timer_CC			
5	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR)) CANCEL Timer_CC	BGAK_R_GEN	(P)	(s10)
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?BGREJ CANCEL Timer_CC	BGREJ_R_GEN	(P)	(s1)
9		+S1_VERIFY			
10		+postamble			
11		LT_PCO?MD	MD_R_GEN		
12		GOTO LB1			
13		LT_PCO?UD	UD_R_GEN		
14		GOTO LB1			
15		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_V_P3
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT ignores a BGAK PDU and remains at state 4.
Configuration :
Default :
Comments : Fig. 20(14 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGAK	BGAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_V_P4

Group : PC/STATE_4/VAL/

Purpose : Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 4.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(15 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S4_V_P5					
Group : PC/STATE_4/VAL/					
Purpose : Verify that the IUT sends a ENDAK PDU on reception of a END PDU at state 4.					
Configuration :					
Default :					
Comments : Ref. 5.0 g, Fig. 20(15 of 51)/PICS PC8					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!ENDPDU	END_S_USER		
3		START Timer_CC			
4	LB1	LT_PCO?ENDAK CANCEL Timer_CC	ENDAK_R_GEN	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S4_V_P6
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT goes to state 1 on reception of ENDAK PDU at state 4.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(15 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!ENDAK	ENDAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_V_P8

Group : PC/STATE_4/VAL/

Purpose : Verify that the IUT ignores a RS PDU and remains at state 4.

Configuration :

Default :

Comments : Fig. 20(16 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!RS	RS_S_GEN(VT_SQ,VR_MR)		
4		START Timer_CC			
5	LB1	?TIMEOUT Timer_CC		(P)	
6		(VT_SQ:=VT_SQ−1)			
7		+S4_VERIFY			
8		+postamble			
9		LT_PCO?ENDPDU	END_R_USER		
10		GOTO LB1			
11		LT_PCO?MD	MD_R_GEN		
12		GOTO LB1			
13		LT_PCO?UD	UD_R_GEN		
14		GOTO LB1			
15		LT_PCO?OTHERWISE		(F)	
16		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_V_P9

Group : PC/STATE_4/VAL/

Purpose : Verify that the IUT ignores a RSAK PDU and remains at state 4.

Configuration :

Default :

Comments : Fig. 20(16 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!RSAK	RSAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_V_P10

Group : PC/STATE_4/VAL/

Purpose : Verify that the IUT ignores a ER PDU and remains at state 4.

Configuration :

Default :

Comments : Fig. 20(16 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!ER	ER_S_GEN(VT_SQ,VR_MR)		
4		START Timer_CC			
5	LB1	?TIMEOUT Timer_CC		(P)	
6		(VT_SQ:=VT_SQ−1)			
7		+S4_VERIFY			
8		+postamble			
9		LT_PCO?ENDPDU	END_R_USER		
10		GOTO LB1			
11		LT_PCO?MD	MD_R_GEN		
12		GOTO LB1			
13		LT_PCO?UD	UD_R_GEN		
14		GOTO LB1			
15		LT_PCO?OTHERWISE		(F)	
16		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_V_P11
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT ignores a ERAK PDU and remains at state 4.
Configuration :
Default :
Comments : Fig. 20(15 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!ERAK	ERAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_V_P12
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT ignores a SD PDU and remains at state 4.
Configuration :
Default :
Comments : Fig. 20(14 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN(VT_S)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_V_P13
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT ignores a POLL PDU and remains at state 4.
Configuration :
Default :
Comments : Fig. 20(14 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(VT_PS:=INC_MOD_24(VT_PS,1))			
3		LT_PCO!POLL	POLL_S_GEN(VT_PS,VT_S)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_V_P14
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT ignores a STAT PDU and remains at state 4.
Configuration :
Default :
Comments : Fig. 20(14 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!STAT	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_MR,VR_R)		list_length=0 no POLL PDU for TCV_N_PS
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_V_P15

Group : PC/STATE_4/VAL/

Purpose : Verify that the IUT ignores a USTAT PDU and remains at state 4.

Configuration :

Default :

Comments : Fig. 20(14 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!USTAT	USTAT_S_LIST(1,3,VR_MR, 1)		elements have no meaning
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_V_P16
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT accepts a UD PDU at state 4.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.2

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!UD	UD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_V_P17
Group : PC/STATE_4/VAL/
Purpose : Verify that the IUT accepts a MD PDU at state 4.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!MD	MD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S4_IV_I1					
Group : PC/STATE_4/INV/					
Purpose : Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 4.					
Configuration :					
Default :					
Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:= GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_INV(VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		(VT_SQ:=VT_SQ−1)			
7		+S4_VERIFY			
8		+postamble			
9		LT_PCO?ENDPDU	END_R_USER		
10		GOTO LB1			
11		LT_PCO?MD	MD_R_GEN		
12		GOTO LB1			
13		LT_PCO?UD	UD_R_GEN		
14		GOTO LB1			
15		LT_PCO?OTHERWISE		(F)	
16		+postamble			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGAK	BGAK_S_INV(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I3
Group : PC/STATE_4/INV/
Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 4.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I4
Group : PC/STATE_4/INV/
Purpose : Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 4.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!ENDPDU	END_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I6
Group : PC/STATE_4/INV/
Purpose : Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 4.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!RS	RS_S_INV(VT_SQ,VR_MR)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I10
Group : PC/STATE_4/INV/
Purpose : Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 4.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!SD	SD_S_INV(VT_S)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I14
Group : PC/STATE_4/INV/
Purpose : Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 4.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!UD	UD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I15

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!MD	MD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I16

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR :=GET_VR_MR())			
4		LT_PCO!IVBGN	IVBGN_S_INV(TCV_OCT,VT_SQ,VR_MR)		
5		START T_Wait			
6	LB1	?TIMEOUT T_Wait		(P)	
7		(VT_SQ:=VT_SQ−1)			
8		+S4_VERIFY			
9		+postamble			
10		LT_PCO?ENDPDU	END_R_USER		
11		GOTO LB1			
12		LT_PCO?MD	MD_R_GEN		
13		GOTO LB1			
14		LT_PCO?UD	UD_R_GEN		
15		GOTO LB1			
16		LT_PCO?OTHERWISE		(F)	
17		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I17

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		(VR_MR:=GET_VR_MR())			
4		LT_PCO!IVBGAK	IVBGAK_S_INV(TCV_OCT, VR_MR)		
5		START T_Wait			
6	LB1	?TIMEOUT T_Wait		(P)	
7		+S4_VERIFY			
8		+postamble			
9		LT_PCO?ENDPDU	END_R_USER		
10		GOTO LB1			
11		LT_PCO?MD	MD_R_GEN		
12		GOTO LB1			
13		LT_PCO?UD	UD_R_GEN		
14		GOTO LB1			
15		LT_PCO?OTHERWISE		(F)	
16		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I18

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGREJ	IVBGREJ_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I19

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVEND	IVEND_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I20_1

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('00000000'O)		extra 4 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I20_2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('0000'O)		extra 2 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I21

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVRS	IVRS_S_INV(TCV_OCT,VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I22_1

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('00000000' O,VR_MR)		extra 4 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I22_2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('0000'O,VR_MR)		extra 2 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I23_1

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('00000000'O,VT_SQ,VR_MR)		extra 4 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I23_2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('0000'O,VT_SQ,VR_MR)		extra 2 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I24_1

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('00000000' O,VR_MR)		extra 4 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I24_2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('0000'O,VR_MR)		extra 2 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I25

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSD	IVSD_S_INV(TCV_OCT,VT_S)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I26_1

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('00000000' O,VT_PS,VT_S)		extra 4 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I26_2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('0000'O,VT_PS,VT_S)		extra 2 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I27_1

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_OCT,'00000000'O,VT_PS,VR_MR, VR_R)		extra 4 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I27_2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_OCT,'0000'O,VT_PS,VR_MR,VR_R)		extra 2 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I28_1

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'00000000'O,VR_MR,VR_R)		extra 4 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I28_2

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTST PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'0000'O,VR_MR,VR_R)		extra 2 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?ENDPDU	END_R_USER		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I29

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVUD	IVUD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I30

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVMD	IVMD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_IV_I31

Group : PC/STATE_4/INV/

Purpose : Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 4.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_CODE(VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S4_VERIFY			
7		+postamble			
8		LT_PCO?ENDPDU	END_R_USER		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_V_A3
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT generates the END PDU on demand at state 5.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(18 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		<IUT!ENDPDU>	END_R_USER		
3		START T_Opr			
4	LB1	LT_PCO?ENDPDU CANCEL T_Opr	END_R_USER	(P)	
5		+S4_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?RS	RS_R_RET(VR_SQ,VT_MS)		
12		GOTO LB1			
13		+TS_Opr			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_V_P1

Group : PC/STATE_5/VAL/

Purpose : Verify that the IUT sends a BGAK and RS PDU on reception of retransmitted BGN PDU at state 5

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(17 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		N(SQ)=VR(SQ)
4		START Timer_CC			
5	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR)) CANCEL Timer_CC	BGAK_R_GEN		
6		START T_Wait			
7	LB2	LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ), VT_MS:=BIT_TO_INT(RS.N_MR)) CANCEL T_Wait	RS_R_RET(VR_SQ,VT_MS)	(P)	
8		+S5_VERIFY			
9		+postamble			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB2			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB2			
14		+TS_Wait			
15		LT_PCO?MD	MD_R_GEN		
16		GOTO LB1			
17		LT_PCO?UD	UD_R_GEN		
18		GOTO LB1			
19		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_V_P2

Group : PC/STATE_5/VAL/

Purpose : Verify that the IUT goes to state 3 on reception of BGN PDU at state 5.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(17 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		N(SQ)<>VR(SQ) (s3)
4		START Timer_CC			
5	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR)) CANCEL Timer_CC	BGAK_R_GEN	(P)	(s10)
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?BGREJ CANCEL Timer_CC	BGREJ_R_GEN	(P)	(s1)
9		+S1_VERIFY			
10		+postamble			
11		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
12		GOTO LB1			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB1			
15		LT_PCO?UD	UD_R_GEN		
16		GOTO LB1			
17		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_V_P3

Group : PC/STATE_5/VAL/

Purpose : Verify that the IUT ignores a BGAK PDU and remains at state 5.

Configuration :

Default :

Comments : Fig. 20(19 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGAK	BGAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_V_P5

Group : PC/STATE_5/VAL/

Purpose : Verify that the IUT sends a ENDAK PDU on reception of a END PDU at state 5.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(17 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!ENDPDU	END_S_USER		
3		START Timer_CC			
4	LB1	LT_PCO?ENDAK CANCEL Timer_CC	ENDAK_R_GEN	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S5_V_P7					
Group : PC/STATE_5/VAL/					
Purpose : Verify that the IUT ignores a retransmitted RS PDU and remains at state 5.					
Configuration :					
Default :					
Comments : Fig. 20(19 of 51)					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!RS	RS_S_GEN(VT_SQ,VR_MR)		N(SQ)=VR(SQ)
4		START Timer_CC			
5	LB1	?TIMEOUT Timer_CC		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S5_V_P8

Group : PC/STATE_5/VAL/

Purpose : Verify that the IUT sends a RSAK PDU on reception of RS PDU and goes to state 10.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(19 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!RS	RS_S_GEN(VT_SQ,VR_MR)		N(SQ)<>VR(SQ)
4		START Timer_CC			
5	LB1	LT_PCO?RSAK(VT_MS:=BIT_TO_INT(RSAK.N_MR)) CANCEL Timer_CC	RSAK_R_GEN	(P)	assume a AA−RESYNC.response from SSCF UNI
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_V_P9

Group : PC/STATE_5/VAL/

Purpose : Verify that the IUT goes to state 10 on reception of RSAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(19 of 51)/PICS PC6

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!RSAK	RSAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?POLL	POLL_R_GEN		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_V_P10

Group : PC/STATE_5/VAL/

Purpose : Verify that the IUT ignores a ER PDU and remains at state 5.

Configuration :

Default :

Comments : Fig. 20(17 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!ER	ER_S_GEN(VT_SQ,VR_MR)		
4		START Timer_CC			
5	LB1	?TIMEOUT Timer_CC		(P)	
6		(VT_SQ:=VT_SQ−1)			
7		+S5_VERIFY			
8		+postamble			
9		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
10		GOTO LB1			
11		LT_PCO?MD	MD_R_GEN		
12		GOTO LB1			
13		LT_PCO?UD	UD_R_GEN		
14		GOTO LB1			
15		LT_PCO?RS	RS_R_RET(VR_SQ,VR_MR)		
16		GOTO LB1			
17		LT_PCO?OTHERWISE		(F)	
18		+postamble			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S5_V_P11					
Group : PC/STATE_5/VAL/					
Purpose : Verify that the IUT ignores a ERAK PDU and remains at state 5.					
Configuration :					
Default :					
Comments : Fig. 20(19 of 51)					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!ERAK	ERAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S5_V_P12
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT ignores a SD PDU and remains at state 5.
Configuration :
Default :
Comments : Fig. 20(19 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN(VT_S)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_V_P13
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT ignores a POLL PDU and remains at state 5.
Configuration :
Default :
Comments : Fig. 20(17 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(VT_PS:=INC_MOD_24(VT_PS,1))			
3		LT_PCO!POLL	POLL_S_GEN(VT_PS,VT_S)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_V_P14

Group : PC/STATE_5/VAL/

Purpose : Verify that the IUT ignores a STAT PDU and remains at state 5.

Configuration :

Default :

Comments : Fig. 20(18 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!STAT	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_MR,VR_R)		list_length=0 no POLL PDU for TCV_N_PS
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S5_V_P15					
Group : PC/STATE_5/VAL/					
Purpose : Verify that the IUT ignores a USTAT PDU and remains at state 5.					
Configuration :					
Default :					
Comments : Fig. 20(18 of 51)					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!USTAT	USTAT_S_LIST(1,3,VR_MR, 1)		elements have no meaning
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S5_V_P16
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT accepts a UD PDU at state 5.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.2

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!UD	UD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments:

Test Case Dynamic Behaviour

Test Case Name: S5_V_P17
Group : PC/STATE_5/VAL/
Purpose : Verify that the IUT accepts a MD PDU at state 5.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!MD	MD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S5_IV_I1					
Group : PC/STATE_5/INV/					
Purpose : Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 5.					
Configuration :					
Default :					
Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_INV(VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		(VT_SQ:=VT_SQ−1)			
7		+S5_VERIFY			
8		+postamble			
9		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
10		GOTO LB1			
11		LT_PCO?MD	MD_R_GEN		
12		GOTO LB1			
13		LT_PCO?UD	UD_R_GEN		
14		GOTO LB1			
15		LT_PCO?OTHERWISE		(F)	
16		+postamble			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I2

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGAK	BGAK_S_INV(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I3

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I4

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!ENDPDU	END_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments:

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I6

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!RS	RS_S_INV(VT_SQ,VR_MR)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I10

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!SD	SD_S_INV(VT_S)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I14
Group : PC/STATE_5/INV/
Purpose : Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 5.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!UD	UD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments:

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I15

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!MD	MD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I16

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR :=GET_VR_MR())			
4		LT_PCO!IVBGN	IVBGN_S_INV(TCV_OCT,VT_SQ,VR_MR)		
5		START T_Wait			
6	LB1	?TIMEOUT T_Wait		(P)	
7		(VT_SQ:=VT_SQ−1)			
8		+S5_VERIFY			
9		+postamble			
10		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
11		GOTO LB1			
12		LT_PCO?MD	MD_R_GEN		
13		GOTO LB1			
14		LT_PCO?UD	UD_R_GEN		
15		GOTO LB1			
16		LT_PCO?OTHERWISE		(F)	
17		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I17

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		(VR_MR:=GET_VR_MR())			
4		LT_PCO!IVBGAK	IVBGAK_S_INV(TCV_OCT, VR_MR)		
5		START T_Wait			
6	LB1	?TIMEOUT T_Wait		(P)	
7		+S5_VERIFY			
8		+postamble			
9		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
10		GOTO LB1			
11		LT_PCO?MD	MD_R_GEN		
12		GOTO LB1			
13		LT_PCO?UD	UD_R_GEN		
14		GOTO LB1			
15		LT_PCO?OTHERWISE		(F)	
16		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I18

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGREJ	IVBGREJ_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I19

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVEND	IVEND_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I20_1

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('00000000'O)		extra 4 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I20_2

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('0000'O)		extra 2 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I21

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVRS	IVRS_S_INV(TCV_OCT,VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I22_1

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('00000000'O,VR_MR)		extra 4 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I22_2

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('0000'O,VR_MR)		extra 2 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I23_1

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('00000000'O,VT_SQ,VR_MR)		extra 4 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I23_2

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('0000'O,VT_SQ,VR_MR)		extra 2 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I24_1

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('00000000'O,VR_MR)		extra 4 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I24_2

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('0000'O,VR_MR)		extra 2 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I25

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSD	IVSD_S_INV(TCV_OCT,VT_S)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I26_1

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('00000000'O,VT_PS,VT_S)		extra 4 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I26_2

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('0000'O,VT_PS,VT_S)		extra 2 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I27_1

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_OCT,'00000000'O,VT_PS,VR_MR, VR_R)		extra 4 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I27_2

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_OCT,'0000'O,VT_PS,VR_MR,VR_R)		extra 2 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I28_1

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'00000000'O,VR_MR,VR_R)		extra 4 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I28_2

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTST PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'0000'O,VR_MR,VR_R)		extra 2 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S5_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I29

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVUD	IVUD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IV_I30

Group : PC/STATE_5/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 5.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVMD	IVMD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S5_IV_I31					
Group : PC/STATE_5/INV/					
Purpose : Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 5.					
Configuration :					
Default :					
Comments : Ref. 7.1, Fig. 20(47 of 51)/PICS PD3					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_CODE(VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S5_VERIFY			
7		+postamble			
8		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S5_IO_P4

Group : PC/STATE_5/INOP/

Purpose : Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 5.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(17 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_IO_P6
Group : PC/STATE_5/INOP/
Purpose : Verify that the IUT goes to state 1 on reception of ENDAK PDU at state 5.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(17 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		LT_PCO!ENDAK	ENDAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ),VT_MS:=BIT_TO_INT(RS.N_MR))	RS_R_RET(VR_SQ,VT_MS)		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments:

Test Case Dynamic Behaviour

Test Case Name: S7_V_P2

Group : PC/STATE_7/VAL/

Purpose : Verify that the IUT goes to state 3 on reception of BGN PDU at state 7.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(25 and 11 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		N(SQ)<>VR(SQ) (s3)
4		+Initialize_State_Variables			
5		START Timer_CC			
6	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR)) CANCEL Timer_CC	BGAK_R_GEN	(P)	assume a AA−ESTABLISH.response from SSCF UNI (s10)
7		+S10_VERIFY			
8		+postamble			
9		LT_PCO?BGREJ CANCEL Timer_CC	BGREJ_R_GEN	(P)	(s1)
10		+S1_VERIFY			
11		+postamble			
12		LT_PCO?MD	MD_R_GEN		
13		GOTO LB1			
14		LT_PCO?UD	UD_R_GEN		
15		GOTO LB1			
16		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_V_P5

Group : PC/STATE_7/VAL/

Purpose : Verify that the IUT sends a ENDAK PDU and goes to state 1 on reception of a END PDU at state 7.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(23 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!ENDPDU	END_S_USER		
3		START Timer_CC			
4	LB1	LT_PCO?ENDAK CANCEL Timer_CC	ENDAK_R_GEN	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_V_P8

Group : PC/STATE_7/VAL/

Purpose : Verify that the IUT goes to state 6 on reception of RS PDU at state 7.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(26 and 11 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!RS	RS_S_GEN(VT_SQ,VR_MR)		N(SQ)<>VR(SQ)
4		+Initialize_State_Variables			
5		START Timer_CC			
6	LB1	LT_PCO?RSAK(VT_MS:=BIT_TO_INT(RSAK.N_MR)) CANCEL Timer_CC	RSAK_R_GEN	(P)	assume a AA−RESYNC.response from SSCF UNI
7		+S10_VERIFY			
8		+postamble			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_V_P11

Group : PC/STATE_7/VAL/

Purpose : Verify that the IUT sends a ERAK PDU and goes to state 8 on reception of a ER PDU at state 7.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(25 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:=GET_VR_MR())			
3		LT_PCO!ER	ER_S_GEN(VT_SQ,VR_MR)		N(SQ)<>VR(SQ)
4		+Initialize_State_Variables			
5		START Timer_CC			
6	LB1	LT_PCO?ERAK(VT_MS:=BIT_TO_INT(ERAK.N_MR)) CANCEL Timer_CC	ERAK_R_GEN	(P)	assume a AA−RECOVER.response from SSCF UNI
7		+S10_VERIFY			
8		+postamble			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_V_P12

Group : PC/STATE_7/VAL/

Purpose : Verify that the IUT goes to state 8 on reception of ERAK PDU at state 7.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(23 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!ERAK	ERAK_S_GEN(VR_MR)		
4		+Initialize_State_Variables			
5		START T_Wait			
6	LB1	?TIMEOUT T_Wait		(P)	
7		+S10_VERIFY			
8		+postamble			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_V_P19
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT ignores a SD PDU and remains at state 7.
Configuration :
Default :
Comments : Fig. 20(25 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN(VT_S)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_V_P21
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT ignores a POLL PDU and remains at state 7.
Configuration :
Default :
Comments : Fig. 20(24 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VT_PS:=INC_MOD_24(VT_PS,1))			
3		LT_PCO!POLL	POLL_S_GEN(VT_PS,VT_S)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_V_P26

Group : PC/STATE_7/VAL/

Purpose : Verify that the IUT ignores a STAT PDU and remains at state 7.

Configuration :

Default :

Comments : Fig. 20(24 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!STAT	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_MR,VR_R)		list_length=0 no POLL PDU for TCV_N_PS
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments:

Test Case Dynamic Behaviour

Test Case Name: S7_V_P36
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT ignores a USTAT PDU and remains at state 7.
Configuration :
Default :
Comments : Fig. 20(24 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!USTAT	USTAT_S_LIST(1,3,VR_MR, 1)		elements have no meaning
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_V_P40
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT accepts a UD PDU at state 7.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.2

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!UD	UD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_V_P41
Group : PC/STATE_7/VAL/
Purpose : Verify that the IUT accepts a MD PDU at state 7.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!MD	MD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:= GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_INV(VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments:

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I2

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGAK	BGAK_S_INV(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I3

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I4

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!ENDPDU	END_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I6

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!RS	RS_S_INV(VT_SQ,VR_MR)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I10

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!SD	SD_S_INV(VT_S)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I14
Group : PC/STATE_7/INV/
Purpose : Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 7.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!UD	UD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I15
Group : PC/STATE_7/INV/
Purpose : Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 7.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!MD	MD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I16

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR :=GET_VR_MR())			
4		LT_PCO!IVBGN	IVBGN_S_INV(TCV_OCT,VT_SQ,VR_MR)		
5		START T_Wait			
6	LB1	?TIMEOUT T_Wait		(P)	
7		+S7_VERIFY			
8		+postamble			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I17

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		(VR_MR:=GET_VR_MR())			
4		LT_PCO!IVBGAK	IVBGAK_S_INV(TCV_OCT, VR_MR)		
5		START T_Wait			
6	LB1	?TIMEOUT T_Wait		(P)	
7		+S7_VERIFY			
8		+postamble			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I18

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGREJ	IVBGREJ_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I19

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVEND	IVEND_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I20_1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('00000000'O)		extra 4 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I20_2

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('0000'O)		extra 2 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I21

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVRS	IVRS_S_INV(TCV_OCT,VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I22_1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('00000000' O,VR_MR)		extra 4 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I22_2

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('0000'O,VR_MR)		extra 2 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I23_1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('00000000'O,VT_SQ,VR_MR)		extra 4 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I23_2

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('0000'O,VT_SQ,VR_MR)		extra 2 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I24_1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('00000000' O,VR_MR)		extra 4 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I24_2

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('0000'O,VR_MR)		extra 2 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I25

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSD	IVSD_S_INV(TCV_OCT,VT_S)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I26_1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('00000000' O,VT_PS,VT_S)		extra 4 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I26_2

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('0000'O,VT_PS,VT_S)		extra 2 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I27_1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_OCT,'00000000'O,VT_PS,VR_MR, VR_R)		extra 4 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I27_2

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_OCT,'0000'O,VT_PS,VR_MR,VR_R)		extra 2 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I28_1

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'00000000'O,VR_MR,VR_R)		extra 4 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I28_2

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTST PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'0000'O,VR_MR,VR_R)		extra 2 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S7_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I29

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVUD	IVUD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I30

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVMD	IVMD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IV_I31

Group : PC/STATE_7/INV/

Purpose : Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 7.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_CODE(VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IO_P1

Group : PC/STATE_7/INOP/

Purpose : Verify that the IUT ignores a retransmitted BGN PDU and remains at state 7.

Configuration :

Default :

Comments : Fig. 20(25 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		N(SQ)=VR(SQ)
4		START Timer_CC			
5	LB1	?TIMEOUT Timer_CC		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?ER	ER_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IO_P3
Group : PC/STATE_7/INOP/
Purpose : Verify that the IUT ignores a BGAK PDU and remains at state 7.
Configuration :
Default :
Comments : Fig. 20(23 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGAK	BGAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IO_P4
Group : PC/STATE_7/INOP/
Purpose : Verify that the IUT goes to state 1 on reception of BGREJ PDU at state 7.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(23 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IO_P6
Group : PC/STATE_7/INOP/
Purpose : Verify that the IUT goes to state 1 on reception of ENDAK PDU at state 7.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(23 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		LT_PCO!ENDAK	ENDAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IO_P7

Group : PC/STATE_7/INOP/

Purpose : Verify that the IUT ignores a retransmitted RS PDU and remains at state 7.

Configuration :

Default :

Comments : Fig. 20(19 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!RS	RS_S_GEN(VT_SQ,VR_MR)		N(SQ)=VR(SQ)
4		START Timer_CC			
5	LB1	?TIMEOUT Timer_CC		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?ER	ER_R_RET(VR_SQ,VT_MS)		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IO_P9

Group : PC/STATE_7/INOP/

Purpose : Verify that the IUT ignores a RSAK PDU and remains at state 7.

Configuration :

Default :

Comments : Fig. 20(23 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!RSAK	RSAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?OTHERWISE		(F)	
13		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_IO_P10

Group : PC/STATE_7/INOP/

Purpose : Verify that the IUT ignores a retransmitted ER PDU and remains at state 7.

Configuration :

Default :

Comments : Fig. 20(25 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!ER	ER_S_GEN(VT_SQ,VR_MR)		N(SQ)=VR(SQ)
4		START Timer_CC			
5	LB1	?TIMEOUT Timer_CC		(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?ER	ER_R_RET(VR_SQ,VT_MS)		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_V_A3
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, generates the END PDU on demand.
Configuration :
Default :
Comments : Ref. 5.0 g, Fig. 20(34 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!ENDPDU>	END_R_USER		
3		START T_Opr			
4	LB1	LT_PCO?ENDPDU CANCEL T_Opr	END_R_USER	(P)	
5		+S4_VERIFY			
6		+postamble			return the IUT in STATE 1
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		+TS_Opr			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_V_A5

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, generates the RS PDU on demand.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(34 of 51)/PICS PC6

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!RS>	RS_R_GEN(VR_SQ)		
3		START T_Opr			
4	LB1	LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ), VT_MS:=BIT_TO_INT(RS.N_MR)) CANCEL T_Opr	RS_R_GEN(VR_SQ)	(P)	
5		+S5_VERIFY			
6		+postamble			return the IUT in STATE 1
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		+TS_Opr			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_V_P1

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a BGAK PDU on reception of a retransmitted BGN PDU.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(35 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		N(SQ)=VR(SQ)
4		START Timer_CC			
5	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR)) CANCEL Timer_CC	BGAK_R_GEN	(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?POLL	POLL_R_GEN		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?POLL	POLL_R_GEN		
15		GOTO LB1			
16		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_V_P2

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, goes to state 3 on reception of BGN PDU.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(35 and 11 of 51)/PICS PC7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		N(SQ)<>VR(SQ)
4		START Timer_CC			
5	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR)) CANCEL Timer_CC	BGAK_R_GEN	(P)	assume a AA−ESTABLISH.response from SSCF UNI
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?BGREJ CANCEL Timer_CC	BGREJ_R_GEN	(P)	(s1)
9		+S1_VERIFY			
10		+postamble			
11		LT_PCO?MD	MD_R_GEN		
12		GOTO LB1			
13		LT_PCO?UD	UD_R_GEN		
14		GOTO LB1			
15		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_V_P3
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, ignores a BGAK PDU and remains.
Configuration :
Default :
Comments : Fig. 20(34 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGAK	BGAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_V_P5

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ENDAK PDU and goes to state 1 on reception of a END PDU.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(36 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!ENDPDU	END_S_USER		
3		START Timer_CC			
4	LB1	LT_PCO?ENDAK CANCEL Timer_CC	ENDAK_R_GEN	(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_V_P7

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a RSAK PDU on reception of a retransmitted RS PDU.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(36 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!RS	RS_S_GEN(VT_SQ,VR_MR)		N(SQ)=VR(SQ)
4		START Timer_CC			
5	LB1	LT_PCO?RSAK(VT_MS:=BIT_TO_INT(RSAK.N_MR)) CANCEL Timer_CC	RSAK_R_GEN	(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?POLL	POLL_R_GEN		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_V_P8

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, goes to state 6 on reception of RS PDU.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(36 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!RS	RS_S_GEN(VT_SQ,VR_MR)		N(SQ)<>VR(SQ)
4		START Timer_CC			
5	LB1	LT_PCO?RSAK(VT_MS:=BIT_TO_INT(RSAK.N_MR)) CANCEL Timer_CC	RSAK_R_GEN	(P)	assume a AA−RESYNC.response from SSCF UNI
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?POLL	POLL_R_GEN		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_V_P9

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, ignores a RSAK PDU and remains.

Configuration :

Default :

Comments : Fig. 20(34 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!RSAK	RSAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_V_P10

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ERAK PDU on reception of a retransmitted ER PDU.

Configuration :

Default :

Comments : Fig. 20(35 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!ER	ER_S_GEN(VT_SQ,VR_MR)		N(SQ)=VR(SQ)
4		START Timer_CC			
5	LB1	LT_PCO?ERAK(VT_MS:=BIT_TO_INT(ERAK.N_MR)) CANCEL Timer_CC	ERAK_R_GEN	(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?POLL	POLL_R_GEN		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_V_P11

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, goes to state 9 on reception of ER PDU.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(35 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
3		LT_PCO!ER	ER_S_GEN(VT_SQ,VR_MR)		N(SQ)<>VR(SQ)
4		START Timer_CC			
5	LB1	LT_PCO?ERAK(VT_MS:=BIT_TO_INT(ERAK.N_MR)) CANCEL Timer_CC	ERAK_R_GEN	(P)	assume a AA−RECOVER.response from SSCF UNI
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?POLL	POLL_R_GEN		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		+TS_CC			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_V_P12
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT, at state 10, ignores a ERAK PDU and remains.
Configuration :
Default :
Comments : Fig. 20(34 of 51)

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!ERAK	ERAK_S_GEN(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S10_V_P13					
Group : PC/STATE_10/VAL/					
Purpose : Verify that the IUT, at state 10, sends a USTAT PDU on reception of SD PDU out of the window.					
Configuration :					
Default :					
Comments : Ref. 5.0 a, h, Fig. 20(40 of 51)/PICS PC5.1					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN(VT_S)		VR(R)=VR(H)=1
3		LT_PCO!SD	SD_S_N_S(VT_MS+2)		SD.N(S)>=VR(MR)
4		START T_Wait			
5	LB1	LT_PCO?USTAT(VT_MS:=BIT_TO_INT(USTAT.N_MR)) CANCEL T_Wait	USTAT_R_LIST(VT_S+1, VT_MS, VT_S+1)	(P)	
6		(VT_S:=VT_MS+2+1)			
7		+S10_VERIFY			
8		+postamble			
9		LT_PCO?POLL	POLL_R_GEN		
10		GOTO LB1			
11		LT_PCO?MD	MD_R_GEN		
12		GOTO LB1			
13		LT_PCO?UD	UD_R_GEN		
14		GOTO LB1			
15		+TS_Wait			
Detailed Comments: SD.N(S)>=VR(MR), VR(H)<VR(MR)					

Test Case Dynamic Behaviour

Test Case Name: S10_V_P14

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, ignores a SD PDU that is out of the window when window is not available.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(40 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN(VT_S)		VR(R)=VR(H)=1
3		LT_PCO!SD	SD_S_N_S(VT_MS+2)		
4		START T_Wait			
5	LB1	LT_PCO?USTAT(VT_MS:=BIT_TO_INT(USTAT.N_MR)) CANCEL T_Wait	USTAT_R_LIST(VT_S+1, VT_MS, VT_S+1)		VR(H)=VR(MR)
6		LT_PCO!SD	SD_S_N_S(VT_MS+2)		SD.N(S)>=VR(MR)
7		START T_Wait			
8	LB2	?TIMEOUT T_Wait		(P)	
9		(VT_S:=VT_MS+2+1)			
10		+S10_VERIFY			
11		+postamble			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB2			
14		LT_PCO?MD	MD_R_GEN		
15		GOTO LB2			
16		LT_PCO?UD	UD_R_GEN		
17		GOTO LB2			
18		LT_PCO?OTHERWISE		(F)	
19		+postamble			
20		LT_PCO?POLL	POLL_R_GEN		
21		GOTO LB1			
22		LT_PCO?MD	MD_R_GEN		
23		GOTO LB1			
24		LT_PCO?UD	UD_R_GEN		
25		GOTO LB1			
26		+TS_Wait			

Detailed Comments: SD.N(S)>=VR(MR), VR(H)>=VR(MR)

Test Case Dynamic Behaviour					
Test Case Name: S10_V_P15					
Group : PC/STATE_10/VAL/					
Purpose : Verify that the IUT, at state 10, saves the next highest expected SD PDU.					
Configuration :					
Default :					
Comments : Ref. 5.0 a, h, Fig. 20(40 of 51)/PICS PC5.1					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_N_S(VT_S+2)		SD.N(S)>VR(H) IUT saves this SD PDU
3		START T_Wait			
4	LB1	LT_PCO?USTAT(VT_MS:=BIT_TO_INT (USTAT.N_MR)) CANCEL T_Wait	USTAT_R_LIST(VT_S, VT_S+2,VT_S)		VR(R)=0, VR(H)=3
5		LT_PCO!SD	SD_S_N_S(VT_S+3)		SD.N(S)=VR(H) IUT saves this SD PDU
6		LT_PCO!SD	SD_S_N_S(VT_S)		IUT indicate PDU(0) VR(R)=1, VR(H)=4
7		LT_PCO!SD	SD_S_N_S(VT_S+1)		IUT indicate PDUs(1,2,3) VR(R)=4, VR(H)=4
8		(VT_PS:=INC_MOD_24(VT_PS, 1))			
9		LT_PCO!POLL	POLL_S_N_S(VT_PS,VT_S +4)		
10		START T_Wait			
11	LB2	LT_PCO?STAT[CHECK_N _PS(VT_PA,BIT_TO_INT(S TAT.N_PS),VT_PS)](VT_M S:=BIT_TO_INT(STAT.N_M R)) CANCEL T_Wait	STAT_R_N_R(VT_S+4)	(P)	list_length=0
12		(VT_S:=5)			
13		+S10_VERIFY			
14		+postamble			
15		LT_PCO?POLL	POLL_R_GEN		
16		GOTO LB2			
17		LT_PCO?MD	MD_R_GEN		
18		GOTO LB2			
19		LT_PCO?UD	UD_R_GEN		
20		GOTO LB2			

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Test Case Dynamic Behaviour					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
21		+TS_Wait			
22		LT_PCO?POLL	POLL_R_GEN		
23		GOTO LB1			
24		LT_PCO?MD	MD_R_GEN		
25		GOTO LB1			
26		LT_PCO?UD	UD_R_GEN		
27		GOTO LB1			
28		+TS_Wait			
Detailed Comments: SD.N(S)<VR(MR), SD.N(S)<>VR(R),SD.N(S)=VR(H)					

Test Case Dynamic Behaviour

Test Case Name: S10_V_P17

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, saves a SD PDU that sequence number is between the sequence number of the next in sequence and the next highest expected SD PDUs.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(40 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_N_S(VT_S+2)		SD.N(S)>VR(H) IUT saves this SD PDU
3		START T_Wait			
4	LB1	LT_PCO?USTAT(VT_MS:=BIT_TO_INT (USTAT.N_MR)) CANCEL T_Wait	USTAT_R_LIST(VT_S, VT_S+2,VT_S)		VR(R)=0, VR(H)=3
5		LT_PCO!SD	SD_S_N_S(VT_S+1)		SD.N(S)<VR(H) IUT saves this SD PDU
6		LT_PCO!SD	SD_S_N_S(VT_S)		IUT indicate PDU(0,1,2) VR(R)=3, VR(H)=3
7		(VT_PS:=INC_MOD_24(VT_PS,1))			
8		LT_PCO!POLL	POLL_S_N_S(VT_PS,VT_S +3)		
9		START T_Wait			
10	LB2	LT_PCO?STAT[CHECK_N_P S(VT_PA,BIT_TO_INT(STAT. N_PS),VT_PS)](VT_MS:=BIT _TO_INT(STAT.N_MR)) CANCEL T_Wait	STAT_R_N_R(VT_S+3)	(P)	list_length=0
11		(VT_S:=4)			
12		+S10_VERIFY			
13		+postamble			
14		LT_PCO?POLL	POLL_R_GEN		
15		GOTO LB2			
16		LT_PCO?MD	MD_R_GEN		
17		GOTO LB2			
18		LT_PCO?UD	UD_R_GEN		
19		GOTO LB2			
20		+TS_Wait			
21		LT_PCO?POLL	POLL_R_GEN		
22		GOTO LB1			

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Test Case Dynamic Behaviour					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
23		LT_PCO?MD	MD_R_GEN		
24		GOTO LB1			
25		LT_PCO?UD	UD_R_GEN		
26		GOTO LB1			
27		+TS_Wait			
Detailed Comments: SD.N(S)<VR(MR), SD.N(S)<>VR(R), SD.N(S)<VR(H), SD.N(S) not in RX BUFFER					

Test Case Dynamic Behaviour

Test Case Name: S10_V_P18

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ER PDU on reception of a SD PDU that sequence number is between the sequence number of the next in sequence and the next highest expected SD PDUs and is already in RX BUFFER.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(40 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_N_S(VT_S+2)		SD.N(S)>VR(H) IUT saves this SD PDU
3		START T_Wait			
4	LB1	LT_PCO?USTAT(VT_MS:=BIT_TO_INT (USTAT.N_MR)) CANCEL T_Wait	USTAT_R_LIST(VT_S, VT_S+2, VT_S)		VR(R)=0, VR(H)=3
5		LT_PCO!SD	SD_S_N_S(VT_S+2)		SD.N(S)<VR(H) this PDU is already in RX BUFFER
6		START T_Wait			
7	LB2	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR)) CANCEL T_Wait	ER_R_GEN(VR_SQ)	(P)	
8		+S7_VERIFY			
9		+postamble			
10		LT_PCO?POLL	POLL_R_GEN		
11		GOTO LB2			
12		LT_PCO?MD	MD_R_GEN		
13		GOTO LB2			
14		LT_PCO?UD	UD_R_GEN		
15		GOTO LB2			
16		+TS_Wait			
17		LT_PCO?POLL	POLL_R_GEN		
18		GOTO LB1			
19		LT_PCO?MD	MD_R_GEN		
20		GOTO LB1			
21		LT_PCO?UD	UD_R_GEN		
22		GOTO LB1			
23		+TS_Wait			

Detailed Comments: SD.N(S)<VR(MR), SD.N(S)<>VR(R), SD.N(S)<VR(H), SD.N(S) in RX BUFFER

Test Case Dynamic Behaviour

Test Case Name: S10_V_P19

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, accepts the next in sequence SD PDU.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(40 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN(VT_S)		SD.N(S)=VR(R)=VR(H)
3		(VT_S:=INC_MOD_24(VT_S,1))			
4		LT_PCO!SD	SD_S_GEN(VT_S)		SD.N(S)=VR(R)=VR(H)
5		(VT_S:=INC_MOD_24(VT_S,1),VT_PS:=INC_MOD_24(VT_PS,1))			
6		LT_PCO!POLL	POLL_S_GEN(VT_PS,VT_S)		
7		START T_Wait			
8	LB1	LT_PCO?STAT[CHECK_N_PS(VT_PA,BIT_TO_INT(STAT.N_PS),VT_PS)](VT_MS:=BIT_TO_INT(STAT.N_MR)) CANCEL T_Wait	STAT_R_N_R(VT_S)	(P)	list_length=0
9		+S10_VERIFY			
10		+postamble			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB1			
15		LT_PCO?UD	UD_R_GEN		
16		GOTO LB1			
17		+TS_Wait			

Detailed Comments: SD.N(S)<VR(MR), SD.N(S)=VR(R)=VR(H)

Test Case Dynamic Behaviour

Test Case Name: S10_V_P21

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ER PDU on reception of a POLL PDU that sequence number is less than that of the next highest expected SD PDU.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(41 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN(VT_S)		VT_S=0
3		(VT_S:=INC_MOD_24(VT_S,1))			
4		LT_PCO!SD	SD_S_GEN(VT_S)		VT_S=1
5		(VT_S:=INC_MOD_24(VT_S,1),VT_PS:=INC_MOD_24(VT_PS,1))			
6		LT_PCO!POLL	POLL_S_N_S(VT_PS,VT_S−2)		POLL.N(S)<VR(H)
7		START T_Wait			
8	LB1	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR)) CANCEL T_Wait	ER_R_GEN(VR_SQ)	(P)	
9		+S7_VERIFY			
10		+postamble			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB1			
15		LT_PCO?UD	UD_R_GEN		
16		GOTO LB1			
17		+TS_Wait			

Detailed Comments: POLL.N(S)<VR(H)

Test Case Dynamic Behaviour

Test Case Name: S10_V_P22

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a STAT PDU on reception of a POLL PDU that sequence number is greater than that of the next highest expected SD PDU and is out of the window.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(41 and 42 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(VT_PS:=INC_MOD_24(VT_PS,1))			
3		LT_PCO!POLL	POLL_S_N_S(VT_PS,VT_MS+2)		POLL.N(S)>=VR(H),POLL.N(S)>VR(MR),VR(R)=VR(H)
4		START T_Wait			
5		(TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S), TCV_LIST:=APPEND_LIST(TCV_LIST,VT_MS)) CANCEL T_Wait			
6	LB1	LT_PCO?STAT[CHECK_N_PS(VT_PA,BIT_TO_INT(STAT.N_PS),VT_PS)]	STAT_R_LIST(TCV_LIST, VT_S)	(P)	
7		(VT_S:=VT_MS+2+1)			
8		+S10_VERIFY			
9		+postamble			
10		LT_PCO?POLL	POLL_R_GEN		
11		GOTO LB1			
12		LT_PCO?MD	MD_R_GEN		
13		GOTO LB1			
14		LT_PCO?UD	UD_R_GEN		
15		GOTO LB1			
16		+TS_Wait			

Detailed Comments: POLL.N(S)>=VR(H), POLL.N(S)>VR(MR), VR(R)=VR(H)

Test Case Dynamic Behaviour

Test Case Name: S10_V_P23_1

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a STAT PDU on reception of a POLL PDU that sequence number is greater than that of the next highest expected SD PDU and is out of the window.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(41and 42 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN(VT_S)		send SD(0)
3		(VT_S:=INC_MOD_24(VT_S,1))			
4		LT_PCO!SD	SD_S_N_S(VT_S+3)		send SD(4)
5		START T_Wait			
6	LB1	LT_PCO?USTAT CANCEL T_Wait	USTAT_R_LIST(VT_S,VT_S+3,VT_S)		
7		(TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S), TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S+3), TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S+4))			element1=1 element2=4 element3=5
8		(VT_PS:=INC_MOD_24(VT_PS,1))			
9		LT_PCO!POLL	POLL_S_N_S(VT_PS,VT_S+4)		POLL(5)
10		START T_Wait			
11	LB2	LT_PCO?STAT[CHECK_N_PS(VT_PA,BIT_TO_INT(STAT.N_PS),VT_PS)] CANCEL T_Wait	STAT_R_LIST(TCV_LIST, VT_S)	(P)	
12		(VT_S:=VT_S+4+1)			
13		+S10_VERIFY			
14		+postamble			
15		LT_PCO?POLL	POLL_R_GEN		
16		GOTO LB2			
17		LT_PCO?MD	MD_R_GEN		
18		GOTO LB2			
19		LT_PCO?UD	UD_R_GEN		
20		GOTO LB2			
21		+TS_Wait			
22		LT_PCO?POLL	POLL_R_GEN		
23		GOTO LB1			
24		LT_PCO?MD	MD_R_GEN		

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Test Case Dynamic Behaviour					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
25		GOTO LB1			
26		LT_PCO?UD	UD_R_GEN		
27		GOTO LB1			
28		+TS_Wait			
Detailed Comments: POLL.N(S)>=VR(H), POLL.N(S)>VR(MR), VR(R)<VR(H)					

Test Case Dynamic Behaviour

Test Case Name: S10_V_P23_2

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a STAT PDUs(with segmenting) on reception of a POLL PDU that sequence number is greater than that of the next highest expected SD PDU and is out of the window.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(41 and 42 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(count:=0)			
3		LT_PCO!SD	SD_S_GEN(VT_S)		send SD(0)
4		(TCV_LIST:=APPEND_LIST(TCV_LIST, VT_S+1), count:=count+1)			LE=1
5	LB1	(VT_S:=INC_MOD_24(VT_S,2))			
6		LT_PCO!SD	SD_S_GEN(VT_S)		send SD(2,4,...)
7		START T_Wait			
8	LB4	LT_PCO?USTAT CANCEL T_Wait	USTAT_R_LIST(VT_S−1, VT_S,1)		
9		(TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S), TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S+1))			LE=2,4, ... LE=3,5, ...
10		(count:=count+2)			
11		[count<Max_STAT]			
12		GOTO LB1			
13		[count>=Max_STAT]			
14		(VT_S:=INC_MOD_24(VT_S,2))			
15		LT_PCO!SD	SD_S_GEN(VT_S)		send SD(x+2)
16		START T_Wait			
17	LB5	LT_PCO?USTAT CANCEL T_Wait	USTAT_R_LIST(VT_S−1, VT_S, 1)		
18		(TCV_LIST1:=APPEND_LIST(TCV_LIST1,VT_S), TCV_LIST1:=APPEND_LIST(TCV_LIST1,VT_S+1), TCV_LIST1:=APPEND_LIST(TCV_LIST1,VT_S+2))			LE=X+1 LE=x+2 LE=VT_MS

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Test Case Dynamic Behaviour					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
19		(VT_PS:=INC_MOD_24(VT_PS,1))			
20		LT_PCO!POLL	POLL_S_N_S(VT_PS,VT_S+2)		
21		START T_Wait			
22	LB2	LT_PCO?STAT[CHECK_N_PS(VT_PA,BIT_TO_INT(STAT.N_PS),VT_PS)] CANCEL T_Wait	STAT_R_LIST(TCV_LIST,1)		
23		START T_Wait			
24	LB3	LT_PCO?STAT[CHECK_N_PS(VT_PA,BIT_TO_INT(STAT.N_PS),VT_PS)] CANCEL T_Wait	STAT_R_LIST(TCV_LIST1,1)	(P)	
25		+RESTORE_SEQUENCE			
26		(VT_S:=VT_S+2+1)			
27		+S10_VERIFY			

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Test Case Dynamic Behaviour					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
28		+postamble			
29		LT_PCO?POLL	POLL_R_GEN		
30		GOTO LB3			
31		LT_PCO?MD	MD_R_GEN		
32		GOTO LB3			
33		LT_PCO?UD	UD_R_GEN		
34		GOTO LB3			
35		+TS_Wait			
36		LT_PCO?POLL	POLL_R_GEN		
37		GOTO LB2			
38		LT_PCO?MD	MD_R_GEN		
39		GOTO LB2			
40		LT_PCO?UD	UD_R_GEN		
41		GOTO LB2			
42		LT_PCO?USTAT	USTAT_R_LIST(VT_S−1, VT_S, 1)		
43		GOTO LB2			
44		+TS_Wait			
45		LT_PCO?POLL	POLL_R_GEN		
46		GOTO LB5			
47		LT_PCO?MD	MD_R_GEN		
48		GOTO LB5			

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Test Case Dynamic Behaviour					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
49		LT_PCO?UD	UD_R_GEN		
50		GOTO LB5			
51		+TS_Wait			
52		LT_PCO?POLL	POLL_R_GEN		
53		GOTO LB4			
54		LT_PCO?MD	MD_R_GEN		
55		GOTO LB4			
56		LT_PCO?UD	UD_R_GEN		
57		GOTO LB4			
58		LT_PCO?OTHERWISE		(I)	
59		+postamble			
60		?TIMEOUT T_Wait		(F)	
61		+postamble			
Detailed Comments POLL.N(S)>=VR(H), POLL.N(S)>VR(MR), VR(R)<VR(H)					

Test Case Dynamic Behaviour

Test Case Name: S10_V_P24

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10 and having no missing gap of received SD PDUs, sends a STAT PDU on reception of a POLL PDU that sequence number is less than or equal to that of the next highest expected SD PDU and is within the window.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(41 and 42 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN(VT_S)		send SD(0)
3		LT_PCO!SD	SD_S_N_S(VT_S+1)		send SD(1)
4		LT_PCO!SD	SD_S_N_S(VT_S+2)		send SD(2)
5		(VT_PS:=INC_MOD_24(VT_PS,1))			
6		LT_PCO!POLL	POLL_S_N_S(VT_PS,VT_S+3)		POLL.N(S)>=VR(H),POLL.N(S),=VR(MR),VR(R)=VR(H)
7		START T_Wait			
8	LB1	LT_PCO?STAT[CHECK_N_PS(VT_PA,BIT_TO_INT(STAT.N_PS),VT_PS)] CANCEL T_Wait	STAT_R_N_R(VT_S+3)	(P)	STAT.LIST=null STAT.N_R=3
9		(VT_S:=VT_S+3+1)			
10		+S10_VERIFY			
11		+postamble			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?MD	MD_R_GEN		
15		GOTO LB1			
16		LT_PCO?UD	UD_R_GEN		
17		GOTO LB1			
18		+TS_Wait			

Detailed Comments: POLL.N(S)>=VR(H), POLL.N(S)<=VR(MR), VR(R)=VR(H)

Test Case Dynamic Behaviour

Test Case Name: S10_V_P25

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10 and having a missing gap of received SD PDU, sends a STAT PDU on reception of a POLL PDU that sequence number is less than or equal to that of the next highest expected SD PDU and is within the window.

Configuration :

Default :

Comments : Ref. 5.0 a, h, Fig. 20(41 and 42 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN(VT_S)		send SD(0)
3		LT_PCO!SD	SD_S_N_S(VT_S+1)		send SD(1)
4		LT_PCO!SD	SD_S_N_S(VT_S+3)		send SD(3)
5		START T_Wait			
6	LB1	LT_PCO?USTAT	USTAT_R_LIST(VT_S+2,VT_S+3,VT_S+2)		
7		CANCEL T_Wait			
8		(TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S+3), TCV_LIST:=APPEND_LIST(TCV_LIST,VT_S+4))			LE=X+1 LE=x+2 LE=VT_MS
9		(VT_PS:=INC_MOD_24(VT_PS,1))			
10		LT_PCO!POLL	POLL_S_N_S(VT_PS,VT_S+4)		POLL.N(S)>=VR(H),POLL.N(S),=VR(MR),VR(R)<VR(H)
11		START T_Wait			
12	LB2	LT_PCO?STAT[CHECK_N_PS(VT_PA,BIT_TO_INT(STAT.N_PS),VT_PS)] CANCEL T_Wait	STAT_R_LIST(TCV_LIST,VT_S+2)	(P)	POLL.LIST=null POLL.N_R=3
13		(VT_S:=VT_S+5)			
14		+S10_VERIFY			
15		+postamble			
16		LT_PCO?POLL	POLL_R_GEN		
17		GOTO LB2			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB2			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB2			

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Test Case Dynamic Behaviour					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
22		+TS_Wait			
23		LT_PCO?POLL	POLL_R_GEN		
24		GOTO LB1			
25		LT_PCO?MD	MD_R_GEN		
26		GOTO LB1			
27		LT_PCO?UD	UD_R_GEN		
28		GOTO LB1			
29		+TS_Wait			
Detailed Comments: POLL.N(S)>=VR(H), POLL.N(S)<=VR(MR), VR(R)<VR(H)					

Test Case Dynamic Behaviour

Test Case Name: S10_V_P26

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number is incorrect.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(44 and 41 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			VT(PA)=0 VT(PS)=0
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!STAT	STAT_S_N_PS_N_R(TCV_LIST,3,VR_MR,VR_R)		STAT.N(PS)=3
4		START T_Wait			
5	LB1	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR)) CANCEL T_Wait	ER_R_GEN(VR_SQ)	(P)	
6		+S7_VERIFY			
7		+postamble			
8		LT_PCO?POLL	POLL_R_GEN		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		+TS_Wait			

Detailed Comments not(VT(PA)<=STAT.N(PS)<=VT(PS))

Test Case Dynamic Behaviour

Test Case Name: S10_V_P27

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number is correct but SD PDU sequence number is incorrect.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(44 and 41 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			VT(PA)=0 VT(PS)=0
2		<IUT!POLL>	POLL_R_GEN		VT(PA)=1 VT(PS)=1
3		START T_Opr			
4	LB1	LT_PCO?POLL(TCV_N_PS:=BIT_TO_INT(POLL.N_PS)) CANCEL T_Opr	POLL_R_GEN		
5		(VR_MR:=GET_VR_MR())			
6		LT_PCO!STAT	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_MR,3)		STAT.N(R)=3
7		START T_Wait			
8	LB2	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR)) CANCEL T_Wait	ER_R_GEN(VR_SQ)	(P)	
9		+S7_VERIFY			
10		+postamble			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB2			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB2			
15		LT_PCO?UD	UD_R_GEN		
16		GOTO LB2			
17		+TS_Wait			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB1			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB1			
22		+TS_Opr			

Detailed Comments: VT(PA)<=STAT.N(PS)<=VT(PS), not(VT(A)<=STAT.N(R)<=VT(S))

Test Case Dynamic Behaviour

Test Case Name: S10_V_P32

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number and SD PDU sequence number are correct but its list element has incorrect sequence number.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(44, 45 and 41 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			VT(PA)=0 VT(PS)=0
2		<IUT!POLL>	POLL_R_GEN		VT(PA)=1 VT(PS)=1
3		START T_Opr			
4	LB1	LT_PCO?POLL(TCV_N_PS:=BIT_TO_INT(POLL.N_PS)) CANCEL T_Opr	POLL_R_GEN		
5		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+2), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R+3))			list element has incorrect sequence number(>VT(S))
6		(VR_MR:=GET_VR_MR())			
7		LT_PCO!STAT	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_MR,VR_R)		
8		START T_Wait			
9	LB2	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR)) CANCEL T_Wait	ER_R_GEN(VR_SQ)	(P)	
10		+S7_VERIFY			
11		+postamble			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB2			
14		LT_PCO?MD	MD_R_GEN		
15		GOTO LB2			
16		LT_PCO?UD	UD_R_GEN		
17		GOTO LB2			
18		+TS_Wait			
19		LT_PCO?MD	MD_R_GEN		
20		GOTO LB1			
21		LT_PCO?UD	UD_R_GEN		
22		GOTO LB1			
23		+TS_Opr			

Detailed Comments: VT(PA)<=STAT.N(PS)<=VT(PS), VT(A)<=STAT.N(R)<=VT(S), list element<=VT(S)

Test Case Dynamic Behaviour

Test Case Name: S10_V_P33

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a STAT PDU that poll sequence number and SD PDU sequence number are correct but its list elements are not increasing order.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(44, 45 and 41 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!SD>	SD_R_GEN(VR_R)		
3		START T_Opr			
4	LB1	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1)) CANCEL T_Opr	SD_R_GEN(VR_R)		
5		<IUT!SD>	SD_R_GEN(VR_R)		
6		START T_Opr			
7	LB2	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1)) CANCEL T_Opr	SD_R_GEN(VR_R)		
8		<IUT!SD>	SD_R_GEN(VR_R)		
9		START T_Opr			
10	LB3	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1)) CANCEL T_Opr	SD_R_GEN(VR_R)		
11		<IUT!POLL>	POLL_R_GEN		
12		START T_Opr			
13	LB4	LT_PCO?POLL(TCV_N_PS:=BIT_TO_INT(POLL.N_PS)) CANCEL T_Opr	POLL_R_GEN		
14		(TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R−1), TCV_LIST:=APPEND_LIST(TCV_LIST,VR_R−2))			list elements are not increasing order
15		(VR_MR:=GET_VR_MR())			
16		LT_PCO!STAT	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_MR,VR_R)		
17		START T_Wait			

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Test Case Dynamic Behaviour					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
18	LB5	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR)) CANCEL T_Wait	ER_R_GEN(VR_SQ)	(P)	
19		+S7_VERIFY			
20		+postamble			
21		LT_PCO?POLL	POLL_R_GEN		
22		GOTO LB5			
23		LT_PCO?MD	MD_R_GEN		
24		GOTO LB5			
25		LT_PCO?UD	UD_R_GEN		
26		GOTO LB5			
27		+TS_Wait			
28		LT_PCO?MD	MD_R_GEN		
29		GOTO LB4			
30		LT_PCO?UD	UD_R_GEN		
31		GOTO LB4			
32		+TS_Opr			
33		LT_PCO?POLL	POLL_R_GEN		
34		GOTO LB3			
35		LT_PCO?MD	MD_R_GEN		
36		GOTO LB3			
37		LT_PCO?UD	UD_R_GEN		
38		GOTO LB3			
39		+TS_Opr			
40		LT_PCO?POLL	POLL_R_GEN		
41		GOTO LB2			
42		LT_PCO?MD	MD_R_GEN		
43		GOTO LB2			
44		LT_PCO?UD	UD_R_GEN		
45		GOTO LB2			
46		+TS_Opr			
47		LT_PCO?POLL	POLL_R_GEN		
48		GOTO LB1			
49		LT_PCO?MD	MD_R_GEN		

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Test Case Dynamic Behaviour					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
50		GOTO LB1			
51		LT_PCO?UD	UD_R_GEN		
52		GOTO LB1			
53		+TS_Opr			
Detailed Comments: VT(PA)<=STAT.N(PS)<=VT(PS), VT(A)<=STAT.N(R)<=VT(S), list element n >= list element n+1					

Test Case Dynamic Behaviour

Test Case Name: S10_V_P38_1

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a USTAT PDU that list element has incorrect sequence number.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(43 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!SD>	SD_R_GEN(VR_R)		
3		START T_Opr			
4	LB1	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1)) CANCEL T_Opr	SD_R_GEN(VR_R)		
5		<IUT!SD>	SD_R_GEN(VR_R)		
6		START T_Opr			
7	LB2	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1)) CANCEL T_Opr	SD_R_GEN(VR_R)		
8		<IUT!SD>	SD_R_GEN(VR_R)		
9		START T_Opr			
10	LB3	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1)) CANCEL T_Opr	SD_R_GEN(VR_R)		
11		(VR_MR:=GET_VR_MR())			
12		LT_PCO!USTAT	USTAT_S_LIST(VR_R+1,VR_R+2,VR_MR,VR_R−1)		list element has incorrect sequence number
13		START T_Wait			
14	LB4	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR)) CANCEL T_Wait	ER_R_GEN(VR_SQ)	(P)	
15		+S7_VERIFY			
16		+postamble			
17		LT_PCO?POLL	POLL_R_GEN		
18		GOTO LB4			
19		LT_PCO?MD	MD_R_GEN		
20		GOTO LB4			
21		LT_PCO?UD	UD_R_GEN		
22		GOTO LB4			
23		+TS_Wait			

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Test Case Dynamic Behaviour					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
24		LT_PCO?POLL	POLL_R_GEN		
25		GOTO LB3			
26		LT_PCO?MD	MD_R_GEN		
27		GOTO LB3			
28		LT_PCO?UD	UD_R_GEN		
29		GOTO LB3			
30		+TS_Opr			
31		LT_PCO?POLL	POLL_R_GEN		
32		GOTO LB2			
33		LT_PCO?MD	MD_R_GEN		
34		GOTO LB2			
35		LT_PCO?UD	UD_R_GEN		
36		GOTO LB2			
37		+TS_Opr			
38		LT_PCO?POLL	POLL_R_GEN		
39		GOTO LB1			
40		LT_PCO?MD	MD_R_GEN		
41		GOTO LB1			
42		LT_PCO?UD	UD_R_GEN		
43		GOTO LB1			
44		+TS_Opr			
Detailed Comments: VT(PA)<=STAT.N(PS)<=VT(PS), VT(A)<=STAT.N(R)<=VT(S), list element n >= list element n+1					

Test Case Dynamic Behaviour

Test Case Name: S10_V_P38_2

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a USTAT PDU that list elements are not increasing order.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(43 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!SD>	SD_R_GEN(VR_R)		
3		START T_Opr			
4	LB1	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1)) CANCEL T_Opr	SD_R_GEN(VR_R)		
5		<IUT!SD>	SD_R_GEN(VR_R)		
6		START T_Opr			
7	LB2	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1)) CANCEL T_Opr	SD_R_GEN(VR_R)		
8		<IUT!SD>	SD_R_GEN(VR_R)		
9		START T_Opr			
10	LB3	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1)) CANCEL T_Opr	SD_R_GEN(VR_R)		
11		(VR_MR:=GET_VR_MR())			
12		LT_PCO!USTAT	USTAT_S_LIST(VR_R−1,VR_R−2,VR_MR,VR_R−1)		
13		START T_Wait			
14	LB4	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR)) CANCEL T_Wait	ER_R_GEN(VR_SQ)	(P)	
15		+S7_VERIFY			
16		+postamble			
17		LT_PCO?POLL	POLL_R_GEN		
18		GOTO LB4			
19		LT_PCO?MD	MD_R_GEN		
20		GOTO LB4			
21		LT_PCO?UD	UD_R_GEN		
22		GOTO LB4			
23		+TS_Wait			
24		LT_PCO?POLL	POLL_R_GEN		
25		GOTO LB3			

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Test Case Dynamic Behaviour					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
26		LT_PCO?MD	MD_R_GEN		
27		GOTO LB3			
28		LT_PCO?UD	UD_R_GEN		
29		GOTO LB3			
30		+TS_Opr			
31		LT_PCO?POLL	POLL_R_GEN		
32		GOTO LB2			
33		LT_PCO?MD	MD_R_GEN		
34		GOTO LB2			
35		LT_PCO?UD	UD_R_GEN		
36		GOTO LB2			
37		+TS_Opr			
38		LT_PCO?POLL	POLL_R_GEN		
39		GOTO LB1			
40		LT_PCO?MD	MD_R_GEN		
41		GOTO LB1			
42		LT_PCO?UD	UD_R_GEN		
43		GOTO LB1			
44		+TS_Opr			
Detailed Comments: VT(PA)<=STAT.N(PS)<=VT(PS), VT(A)<=STAT.N(R)<=VT(S), list element n >= list element n+1					

Test Case Dynamic Behaviour

Test Case Name: S10_V_P39

Group : PC/STATE_10/VAL/

Purpose : Verify that the IUT, at state 10, sends a ER PDU and goes to state 7 on reception of a USTAT PDU that SD PDU sequence number is incorrect.

Configuration :

Default :

Comments : Ref. 5.0 i, Fig. 20(43 of 51)/PICS PC5.1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!SD>	SD_R_GEN(VR_R)		
3		START T_Opr			
4	LB1	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1)) CANCEL T_Opr	SD_R_GEN(VR_R)		
5		<IUT!SD>	SD_R_GEN(VR_R)		
6		START T_Opr			
7	LB2	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1)) CANCEL T_Opr	SD_R_GEN(VR_R)		
8		<IUT!SD>	SD_R_GEN(VR_R)		
9		START T_Opr			
10	LB3	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1)) CANCEL T_Opr	SD_R_GEN(VR_R)		
11		(VR_MR:=GET_VR_MR())			
12		LT_PCO!USTAT	USTAT_S_LIST(VR_R−1,VR_R,VR_MR,VR_R+1)		USTAT.N(R) > VT(S)
13		START T_Wait			
14	LB4	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR)) CANCEL T_Wait	ER_R_GEN(VR_SQ)	(P)	
15		+S7_VERIFY			
16		+postamble			
17		LT_PCO?POLL	POLL_R_GEN		
18		GOTO LB4			
19		LT_PCO?MD	MD_R_GEN		
20		GOTO LB4			
21		LT_PCO?UD	UD_R_GEN		
22		GOTO LB4			
23		+TS_Wait			
24		LT_PCO?POLL	POLL_R_GEN		
25		GOTO LB3			

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Test Case Dynamic Behaviour					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
26		LT_PCO?MD	MD_R_GEN		
27		GOTO LB3			
28		LT_PCO?UD	UD_R_GEN		
29		GOTO LB3			
30		+TS_Opr			
31		LT_PCO?POLL	POLL_R_GEN		
32		GOTO LB2			
33		LT_PCO?MD	MD_R_GEN		
34		GOTO LB2			
35		LT_PCO?UD	UD_R_GEN		
36		GOTO LB2			
37		+TS_Opr			
38		LT_PCO?POLL	POLL_R_GEN		
39		GOTO LB1			
40		LT_PCO?MD	MD_R_GEN		
41		GOTO LB1			
42		LT_PCO?UD	UD_R_GEN		
43		GOTO LB1			
44		+TS_Opr			
Detailed Comments: USTAT.N(R) > VT(S)					

Test Case Dynamic Behaviour

Test Case Name: S10_V_P40
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT accepts a UD PDU at state 10.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.2

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!UD	UD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_V_P41
Group : PC/STATE_10/VAL/
Purpose : Verify that the IUT accepts a MD PDU at state 10.
Configuration :
Default :
Comments : Ref 5.0 h, Fig. 20(47 of 51)/PICS PC5.3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!MD	MD_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I1

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is not 32−bit aligned at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR:= GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_INV(VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I2

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid BGAK PDU which is not 32−bit aligned at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGAK	BGAK_S_INV(VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I3

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is not 32−bit aligned at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I4

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is not 32−bit aligned at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!ENDPDU	END_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I6

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid RS PDU which is not 32−bit aligned at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!RS	RS_S_INV(VT_SQ,VR_MR)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I10
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid SD PDU which is not 32−bit aligned at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_INV(VT_S)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I14
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid UD PDU which is not 32−bit aligned at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!UD	UD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I15

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is not 32−bit aligned at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!MD	MD_S_INV		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I16

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid BGN PDU which is 32−bit aligned but is not the proper length of the BGN PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 8, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		(VT_SQ:=INC_MOD_8(VT_SQ,1),VR_MR :=GET_VR_MR())			
4		LT_PCO!IVBGN	IVBGN_S_INV(TCV_OCT,VT_SQ,VR_MR)		
5		START T_Wait			
6	LB1	?TIMEOUT T_Wait		(P)	
7		+S10_VERIFY			
8		+postamble			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?POLL	POLL_R_GEN		
14		GOTO LB1			
15		LT_PCO?OTHERWISE		(F)	
16		+postamble			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S10_IV_I17					
Group : PC/STATE_10/INV/					
Purpose : Verify that the IUT ignores an invalid BGAK PDU which is 32−bit aligned but is not the proper length of the BGAK PDU at state 10.					
Configuration :					
Default :					
Comments : Ref. 7.1, Fig. 9, Fig. 20(47 of 51)/PICS PD3					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		(VR_MR:=GET_VR_MR())			
4		LT_PCO!IVBGAK	IVBGAK_S_INV(TCV_OCT, VR_MR)		
5		START T_Wait			
6	LB1	?TIMEOUT T_Wait		(P)	
7		+S10_VERIFY			
8		+postamble			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?POLL	POLL_R_GEN		
14		GOTO LB1			
15		LT_PCO?OTHERWISE		(F)	
16		+postamble			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I18

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid BGREJ PDU which is 32−bit aligned but is not the proper length of the BGREJ PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 10, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVBGREJ	IVBGREJ_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I19

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid END PDU which is 32−bit aligned but is not the proper length of the END PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 11, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVEND	IVEND_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I20_1

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is 32−bit aligned but is not the proper length of the ENDAK PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('00000000'O)		extra 4 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I20_2

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid ENDAK PDU which is not 32−bit aligned and is not the proper length of the ENDAK PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 12, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVENDAK	IVENDAK_S_INV('0000'O)		extra 2 octets in ENDAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour					
Test Case Name: S10_IV_I21					
Group : PC/STATE_10/INV/					
Purpose : Verify that the IUT ignores an invalid RS PDU which is 32−bit aligned but is not the proper length of the RS PDU at state 10.					
Configuration :					
Default :					
Comments : Ref. 7.1, Fig. 13, Fig. 20(47 of 51)/PICS PD3					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(UU_Max_Len + ((4 − (UU_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (UU_Max_Len + PAD + 4)
3		LT_PCO!IVRS	IVRS_S_INV(TCV_OCT,VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			
Detailed Comments					

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I22_1

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is 32−bit aligned but is not the proper length of the RSAK PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('00000000' O,VR_MR)		extra 4 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I22_2

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid RSAK PDU which is not 32−bit aligned and is not the proper length of the RSAK PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 14, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVRSAK	IVRSAK_S_INV('0000'O,VR_MR)		extra 2 octets in RSAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I23_1

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is 32−bit aligned but is not the proper length of the ER PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('00000000'O,VT_SQ,VR_MR)		extra 4 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I23_2

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid ER PDU which is not 32−bit aligned and is not the proper length of the ER PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 15, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVER	IVER_S_INV('0000'O,VT_SQ,VR_MR)		extra 2 octets in ER PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I24_1

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is 32−bit aligned but is not the proper length of the ERAK PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('00000000' O,VR_MR)		extra 4 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I24_2

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid ERAK PDU which is not 32−bit aligned and is not the proper length of the ERAK PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 16, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVERAK	IVERAK_S_INV('0000'O,VR_MR)		extra 2 octets in ERAK PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I25

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid SD PDU which is 32−bit aligned but is not the proper length of the SD PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 3, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSD	IVSD_S_INV(TCV_OCT,VT_S)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I26_1

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is 32−bit aligned but is not the proper length of the POLL PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('00000000'O,VT_PS,VT_S)		extra 4 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I26_2

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid POLL PDU which is not 32−bit aligned and is not the proper length of the POLL PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 4, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVPOLL	IVPOLL_S_INV('0000'O,VT_PS,VT_S)		extra 2 octets in POLL PDU
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I27_1

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is 32−bit aligned but is not the proper length of the STAT PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_OCT,'00000000'O,VT_PS,VR_MR, VR_R)		extra 4 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I27_2

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid STAT PDU which is not 32−bit aligned and is not the proper length of the STAT PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 5, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVSTAT	IVSTAT_S_INV(TCV_OCT,'0000'O,VT_PS,VR_MR,VR_R)		extra 2 octets in STAT PDU
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I28_1

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is 32−bit aligned but is not the proper length of the USTAT PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'00000000'O,VR_MR,VR_R)		extra 4 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I28_2

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid USTAT PDU which is not 32−bit aligned and is not the proper length of the USTST PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 6, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!IVUSTAT	IVUSTAT_S_INV(VR_R,VR_R+1,'0000'O,VR_MR,VR_R)		extra 2 octets in USTAT PDU. list elements have no meaning
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S10_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?POLL	POLL_R_GEN		
12		GOTO LB1			
13		LT_PCO?OTHERWISE		(F)	
14		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I29

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid UD PDU which is 32−bit aligned but is not the proper length of the UD PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVUD	IVUD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I30

Group : PC/STATE_10/INV/

Purpose : Verify that the IUT ignores an invalid MD PDU which is 32−bit aligned but is not the proper length of the MD PDU at state 10.

Configuration :

Default :

Comments : Ref. 7.1, Fig. 7, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(TCV_OCT:=INT_TO_HEX(0,(Info_Max_Len + ((4 − (Info_Max_Len MOD 4)) MOD 4) + 4)*2))			length = (Info_Max_Len + PAD + 4)
3		LT_PCO!IVMD	IVMD_S_INV(TCV_OCT)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IV_I31
Group : PC/STATE_10/INV/
Purpose : Verify that the IUT ignores an invalid PDU which has an unknown PDU type code at state 10.
Configuration :
Default :
Comments : Ref. 7.1, Fig. 20(47 of 51)/PICS PD3

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(VR_MR:=GET_VR_MR())			
3		LT_PCO!BGN	BGN_S_CODE(VT_SQ,VR_MR)		
4		START T_Wait			
5	LB1	?TIMEOUT T_Wait		(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
14		LT_PCO?OTHERWISE		(F)	
15		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IO_P4

Group : PC/STATE_10/INOP/

Purpose : Verify that the IUT, at state 10, goes to state 1 on reception of BGREJ PDU.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(36 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!BGREJ	BGREJ_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IO_P6

Group : PC/STATE_10/INOP/

Purpose : Verify that the IUT, at state 10, goes to state 1 on reception of ENDAK PDU.

Configuration :

Default :

Comments : Ref. 5.0 g, Fig. 20(36 of 51)/PICS PC8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!ENDAK	ENDAK_S_GEN		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait		(P)	
5		+S1_VERIFY			
6		+postamble			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		LT_PCO?OTHERWISE		(F)	
12		+postamble			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S2_CC_T1

Group : SP/TIMER_TESTS/

Purpose : Verify that the IUT, at state 2, sends a END PDU and goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.

Configuration :

Default :

Comments : Ref. 5.0 g, 7.6 d, Fig. 20(9 of 51)/PICS SP1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S2_PREAMBLE			
2		(count:=1)			
3	LB1	START Timer_CC			
4		?TIMEOUT Timer_CC			
5		START T_Wait			
6	LB2	LT_PCO?BGN	BGN_R_RET(VR_SQ,VT_MS)		identical to the last BGN PDU
7		CANCEL T_Wait			
8		(count:=count+1)			
9		[count < Max_CC]			
10		GOTO LB1			
11		[count >=Max_CC]			
12		START Timer_CC			
13		?TIMEOUT Timer_CC			
14		START T_Wait			
15	LB3	LT_PCO?ENDPDU CANCEL T_Wait	END_R_SSCOP	(P)	
16		+S1_VERIFY			
17		+postamble			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB3			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB3			
22		+TS_Wait			
23		LT_PCO?MD	MD_R_GEN		
24		GOTO LB2			
25		LT_PCO?UD	UD_R_GEN		
26		GOTO LB2			
27		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S4_CC_T1

Group : SP/TIMER_TESTS/

Purpose : Verify that the IUT, at state 4, goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.

Configuration :

Default :

Comments : Ref. 5.0 g, 7.6 d, Fig. 20(15 of 51)/PICS SP1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S4_PREAMBLE			
2		(count:=1)			
3	LB1	START Timer_CC			
4		?TIMEOUT Timer_CC			
5		START T_Wait			
6	LB2	LT_PCO?ENDPDU	END_R_USER		identical to the last END PDU
7		CANCEL T_Wait			
8		(count:=count+1)			
9		[count < Max_CC]			
10		GOTO LB1			
11		[count >=Max_CC]			
12		START Timer_CC			
13		?TIMEOUT Timer_CC			
14		START T_Wait			
15		?TIMEOUT T_Wait			
16		+S1_VERIFY			
17		+postamble			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB2			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB2			
22		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S5_CC_T1

Group : SP/TIMER_TESTS/

Purpose : Verify that the IUT, at state 5, sends a END PDU and goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.

Configuration :

Default :

Comments : Ref. 5.0 g, 7.6 d, Fig. 20(18 of 51)/PICS SP1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S5_PREAMBLE			
2		(count:=1)			
3	LB1	START Timer_CC			
4		?TIMEOUT Timer_CC			
5		START T_Wait			
6	LB2	LT_PCO?RS	RS_R_RET(VR_SQ,VT_MS)		identical to the last RS PDU
7		CANCEL T_Wait			
8		(count:=count+1)			
9		[count < Max_CC]			
10		GOTO LB1			
11		[count >=Max_CC]			
12		START Timer_CC			
13		?TIMEOUT Timer_CC			
14		START T_Wait			
15	LB3	LT_PCO?ENDPDU CANCEL T_Wait	END_R_SSCOP	(P)	
16		+S1_VERIFY			
17		+postamble			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB3			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB3			
22		+TS_Wait			
23		LT_PCO?MD	MD_R_GEN		
24		GOTO LB2			
25		LT_PCO?UD	UD_R_GEN		
26		GOTO LB2			
27		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S7_CC_T1

Group : SP/TIMER_TESTS/

Purpose : Verify that the IUT, at state 7, sends a END PDU and goes to state 1 when the Timer Timer_CC is expired and the value of the connection control state variable exceeds the maximum value.

Configuration :

Default :

Comments : Ref. 5.0 g, 7.6 d, Fig. 20(24 of 51)/PICS SP1

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S7_PREAMBLE			
2		(count:=1)			
3	LB1	START Timer_CC			
4		?TIMEOUT Timer_CC			
5		START T_Wait			
6	LB2	LT_PCO?ER	ER_R_RET(VR_SQ,VT_MS)		identical to the last ER PDU
7		CANCEL T_Wait			
8		(count:=count+1)			
9		[count < Max_CC]			
10		GOTO LB1			
11		[count >=Max_CC]			
12		START Timer_CC			
13		?TIMEOUT Timer_CC			
14		START T_Wait			
15	LB3	LT_PCO?ENDPDU CANCEL T_Wait	END_R_SSCOP	(P)	
16		+S1_VERIFY			
17		+postamble			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB3			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB3			
22		+TS_Wait			
23		LT_PCO?MD	MD_R_GEN		
24		GOTO LB2			
25		LT_PCO?UD	UD_R_GEN		
26		GOTO LB2			
27		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_POLL_T3
Group : SP/TIMER_TESTS/
Purpose : Verify that the IUT, at state 10, sends a POLL PDU when the Timer Timer_POLL is expired .
Configuration :
Default :
Comments : Ref. 7.6 a, Fig. 20(37 of 51)/PICS SP5

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		START Timer_POLL			
3		?TIMEOUT Timer_POLL			
4		START T_Wait			
5	LB1	LT_PCO?POLL CANCEL T_Wait	POLL_R_GEN	(P)	
6		+S10_VERIFY			
7		+postamble			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB1			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB1			
12		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_KEEP_ALIVE_T4

Group : SP/TIMER_TESTS/

Purpose : Verify that the IUT, at state 10, sends a POLL PDU when the Timer Timer_KEEP_ALIVE is expired .

Configuration :

Default :

Comments : Ref. 7.6 b, Fig. 20(37 of 51)/PICS SP6

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		START Timer_POLL			
3		?TIMEOUT Timer_POLL			
4		START T_Wait			
5	LB1	LT_PCO?POLL	POLL_R_GEN		
6		CANCEL T_Wait			
7		START Timer_KEEP_ALIVE			
8		?TIMEOUT Timer_KEEP_ALIVE			
9		START T_Wait			
10	LB2	LT_PCO?POLL CANCEL T_Wait	POLL_R_GEN	(P)	
11		+S10_VERIFY			
12		+postamble			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB2			
15		LT_PCO?UD	UD_R_GEN		
16		GOTO LB2			
17		+TS_Wait			
18		LT_PCO?MD	MD_R_GEN		
19		GOTO LB1			
20		LT_PCO?UD	UD_R_GEN		
21		GOTO LB1			
22		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_IDLE_T5

Group : SP/TIMER_TESTS/

Purpose : Verify that the IUT, at state 10, sends a POLL PDU when the Timer Timer_IDLE is expired .

Configuration :

Default :

Comments : Ref. 7.6 c, Fig. 20(37 of 51)/PICS SP8

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		START Timer_POLL			
3		?TIMEOUT Timer_POLL			
4		START T_Wait			
5	LB1	LT_PCO?POLL(TCV_N_PS:= BIT_TO_INT(POLL.N_PS))	POLL_R_GEN		IUT start Timer_KEEP_ALIVE
6		CANCEL T_Wait			
7		LT_PCO!STAT	STAT_S_N_PS_N_R(TCV_LIST,TCV_N_PS,VR_MR,VR_R)		IUT start Timer_IDLE
8		START Timer_IDLE			
9		?TIMEOUT Timer_IDLE			
10		START T_Wait			
11	LB2	LT_PCO?POLL CANCEL T_Wait	POLL_R_GEN	(P)	
12		+S10_VERIFY			
13		+postamble			
14		LT_PCO?MD	MD_R_GEN		
15		GOTO LB2			
16		LT_PCO?UD	UD_R_GEN		
17		GOTO LB2			
18		+TS_Wait			
19		LT_PCO?MD	MD_R_GEN		
20		GOTO LB1			
21		LT_PCO?UD	UD_R_GEN		
22		GOTO LB1			
23		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: S10_NO_RESPONSE_T6
Group : SP/TIMER_TESTS/
Purpose : Verify that the IUT, at state 10, sends a END PDU when the Timer Timer_NO_RESPONSE is expired .
Configuration :
Default :
Comments : Ref. 7.6 a, Fig. 20(37 of 51)/PICS SP7

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			IUT start Timer_NO_RESPONSE
2		START Timer_NO_RESPONSE			
3		?TIMEOUT Timer_NO_RESPONSE			
4		START T_Wait			
5	LB1	LT_PCO?ENDPDU CANCEL T_Wait	END_R_SSCOP	(P)	
6		+S1_VERIFY			
7		+postamble			
8		LT_PCO?POLL	POLL_R_GEN		
9		GOTO LB1			
10		LT_PCO?MD	MD_R_GEN		
11		GOTO LB1			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		+TS_Wait			

Detailed Comments

Test Case Dynamic Behaviour

Test Case Name: SP3_MaxPD

Group : SP/PARAM/

Purpose : Check the value of MaxPD system parameter(Maximum number of SD PDUs before transmission of a POLL PDU).

Configuration :

Default :

Comments : Ref. 7.7 c/PICS SP2

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		(count:=0)			
3	LB1	<IUT!SD>	SD_R_GEN(VR_R)		
4		START T_Opr			
5	LB2	LT_PCO?SD(VR_R:=INC_MOD_24(VR_R,1)) CANCEL T_Opr	SD_R_GEN(VR_R)		
6		(count:=count+1)			
7		[count>=Max_PD]			
8		LT_PCO?POLL	POLL_R_GEN	(P)	
9		+S10_VERIFY			
10		+postamble			
11		[count<Max_PD]			
12		GOTO LB1			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB2			
15		LT_PCO?UD	UD_R_GEN		
16		GOTO LB2			
17		LT_PCO?POLL	POLL_R_GEN		
18		GOTO LB2			
19		+TS_Opr			

Detailed Comments

Test Step Dynamic Behaviour					
Test Step Name : TS_Wait					
Group : GENERAL/					
Objective : Test Step of alternatives OTHERWISE, and TIMEOUT of T_Wait.					
Default :					
Comments :					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO?OTHERWISE		(F)	
2		+postamble			
3		?TIMEOUT T_Wait		(F)	
4		+postamble			
Detailed Comments					

Test Step Dynamic Behaviour					
Test Step Name : TS_Opr					
Group : GENERAL/					
Objective : Test Step of alternatives OTHERWISE, and TIMEOUT of T_Opr.					
Default :					
Comments :					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO?OTHERWISE		(F)	
2		+postamble			
3		?TIMEOUT T_Opr		(F)	
4		+postamble			
Detailed Comments					

Test Step Dynamic Behaviour					
Test Step Name : TS_CC					
Group : GENERAL/					
Objective : Test Step of alternatives OTHERWISE, and TIMEOUT of Timer_CC.					
Default :					
Comments :					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO?OTHERWISE		(F)	
2		+postamble			
3		?TIMEOUT Timer_CC		(F)	
4		+postamble			
Detailed Comments					

Test Step Dynamic Behaviour					
Test Step Name : RESTORE_SEQUENCE					
Group : GENERAL/					
Objective :					
Default :					
Comments :					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		(VT_S:=VT_S−1)			
2		LT_PCO!SD	SD_S_GEN(VT_S)		
3		START T_Wait			
4	LB1	?TIMEOUT T_Wait			
5		(VT_S:=VT_S−2)			
6		LT_PCO!SD	SD_S_GEN(VT_S)		
7		START T_Wait			
8	LB2	?TIMEOUT T_Wait			
9		(VT_S:=VT_S+3)		(P)	
10		LT_PCO?POLL	POLL_R_GEN		
11		GOTO LB2			
12		LT_PCO?POLL	POLL_R_GEN		
13		GOTO LB1			
Detailed Comments					

Test Step Dynamic Behaviour					
Test Step Name : Initialize_State_Variables					
Group : PROCEDURE/					
Objective : Procedure used to initialize state variables when new connection is established.					
Default :					
Comments :					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		(VT_S:=0, VT_PS:=0, VT_A:=0)			
2		(VT_PA:=1, VT_PD:=0)			
3		(VR_R:=0, VR_H:=0)			
Detailed Comments					

Test Step Dynamic Behaviour

Test Step Name : postamble

Group :

Objective : Procedure used to place the IUT at state 1(IDLE) from any state.

Default :

Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO!BGREJ	BGREJ_S_GEN		
2		START T_Wait			
3	LB1	?TIMEOUT T_Wait			
4		(count:=0)			
5	LB2	LT_PCO!ENDPDU(count:=count+1)	END_S_USER		
6		START Timer_CC			
7	LB3	LT_PCO?ENDAK CANCEL Timer_CC	ENDAK_R_GEN	R	
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB3			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB3			
12		?TIMEOUT Timer_CC			
13		[count < Max_CC]			
14		GOTO LB2			
15		[count >= Max_CC]		I	
16		LT_PCO?OTHERWISE		I	
17		LT_PCO?MD	MD_R_GEN		
18		GOTO LB1			
19		LT_PCO?UD	UD_R_GEN		
20		GOTO LB1			
21		LT_PCO?POLL	POLL_R_GEN		
22		GOTO LB1			
23		LT_PCO?OTHERWISE		I	

Detailed Comments

Test Step Dynamic Behaviour					
Test Step Name : S1_PREAMBLE					
Group : PREAMBLE/					
Objective : Procedure used to place the IUT at state 1(IDLE) from any state.					
Default :					
Comments :					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		LT_PCO!BGREJ	BGREJ_S_GEN		
2		START T_Wait			
3	LB1	?TIMEOUT T_Wait			
4		(count:=0)			
5	LB2	LT_PCO!ENDPDU(count:=count+1)	END_S_USER		
6		START Timer_CC			
7	LB3	LT_PCO?ENDAK CANCEL Timer_CC	ENDAK_R_GEN		
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB3			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB3			
12		?TIMEOUT Timer_CC			
13		[count < Max_CC]			
14		GOTO LB2			
15		[count >= Max_CC]		(I)	
16		+postamble			
17		LT_PCO?OTHERWISE		(I)	
18		+postamble			
19		LT_PCO?MD	MD_R_GEN		
20		GOTO LB1			
21		LT_PCO?UD	UD_R_GEN		
22		GOTO LB1			
23		LT_PCO?OTHERWISE		(I)	
Detailed Comments					

Test Step Dynamic Behaviour

Test Step Name : S2_PREAMBLE

Group : PREAMBLE/

Objective : Procedure used to place the IUT at state 2(OUTGOING CONNECTION PENDING) from any state.

Default :

Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		<IUT!BGN>	BGN_R_GEN(VR_SQ)		
3		START T_Opr			
4	LB1	LT_PCO?BGN(VR_SQ:=BIT_TO_INT(BGN.N_SQ), VT_MS:=BIT_TO_INT(BGN.N_MR)) CANCEL T_Opr	BGN_R_GEN(VR_SQ)		
5		LT_PCO?MD	MD_R_GEN		
6		GOTO LB1			
7		LT_PCO?UD	UD_R_GEN		
8		GOTO LB1			
9		?TIMEOUT T_Opr		(I)	
10		+postamble			
11		LT_PCO?OTHERWISE		(I)	
12		+postamble			

Detailed Comments

Test Step Dynamic Behaviour

Test Step Name : S4_PREAMBLE

Group : PREAMBLE/

Objective : Procedure used to place the IUT at state 4(OUTGOING DISCONNECTION PENDING) from any state.

Default :

Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!ENDPDU>	END_R_USER		
3		START T_Opr			
4	LB1	LT_PCO?ENDPDU CANCEL T_Opr	END_R_USER		
5		LT_PCO?POLL	POLL_R_GEN		
6		GOTO LB1			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		LT_PCO?UD	UD_R_GEN		
10		GOTO LB1			
11		?TIMEOUT T_Opr		(I)	
12		+postamble			
13		LT_PCO?OTHERWISE		(I)	
14		+postamble			

Detailed Comments

Test Step Dynamic Behaviour

Test Step Name : S5_PREAMBLE

Group : PREAMBLE/

Objective : Procedure used to place the IUT at state 5(OUTGOING RESYNCHRONIZATION PENDING) from any state.

Default :

Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		<IUT!RS>	RS_R_GEN(VR_SQ)		
3		START T_Opr			
4	LB1	LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ), VT_MS:=BIT_TO_INT(RS.N_MR)) CANCEL T_Opr	RS_R_GEN(VR_SQ)		
5		LT_PCO?POLL	POLL_R_GEN		
6		GOTO LB1			
7		LT_PCO?UD	UD_R_GEN		
8		GOTO LB1			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB1			
11		?TIMEOUT T_Opr		(I)	
12		+postamble			
13		LT_PCO?OTHERWISE		(I)	
14		+postamble			

Detailed Comments

Test Step Dynamic Behaviour

Test Step Name : S7_PREAMBLE

Group : PREAMBLE/

Objective : Procedure used to place the IUT at state 7(OUTGOING RECOVERY PENDING) from any state.

Default :

Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S10_PREAMBLE			
2		LT_PCO!SD	SD_S_GEN(VT_S)		VT_S=0
3		(VT_S:=INC_MOD_24(VT_S,3))			
4		LT_PCO!SD	SD_S_GEN(VT_S)		VT_S=3
5		(VT_S:=INC_MOD_24(VT_S,1),VT_PS:=INC_MOD_24(VT_PS,1))			
6		LT_PCO!POLL	POLL_S_N_S(VT_PS,VT_S−3)		VR(H)>POLL.N(S)
7		START T_Wait			
8	LB1	LT_PCO?ER(VR_SQ:=BIT_TO_INT(ER.N_SQ), VT_MS:=BIT_TO_INT(ER.N_MR)) CANCEL T_Wait	ER_R_GEN(VR_SQ)		
9		LT_PCO?POLL	POLL_R_GEN		
10		GOTO LB1			
11		LT_PCO?UD	UD_R_GEN		
12		GOTO LB1			
13		LT_PCO?MD	MD_R_GEN		
14		GOTO LB1			
15		LT_PCO?USTAT	USTAT_R_LIST(1, 3,1)		
16		GOTO LB1			
17		?TIMEOUT T_Wait		(I)	
18		+postamble			
19		LT_PCO?OTHERWISE		(I)	
20		+postamble			

Detailed Comments

Test Step Dynamic Behaviour

Test Step Name: S10_PREAMBLE

Group : PREAMBLE/

Objective : Procedure used to place the IUT at state 10(DATA TRANSFER READY) from any state.

Default :

Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		+S1_PREAMBLE			
2		(count:=0)			
3		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
4	LB1	LT_PCO!BGN(count:=count+1)	BGN_S_GEN(VT_SQ,VR_MR)		
5		START Timer_CC			
6	LB2	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR)) CANCEL Timer_CC	BGAK_R_GEN		
7		+Initialize_State_Variables			
8		LT_PCO?MD	MD_R_GEN		
9		GOTO LB2			
10		LT_PCO?UD	UD_R_GEN		
11		GOTO LB2			
12		?TIMEOUT Timer_CC			
13		[count < Max_CC]			
14		GOTO LB1			
15		[count >= Max_CC]		(I)	
16		+postamble			
17		LT_PCO?OTHERWISE		(I)	
18		+postamble			

Detailed Comments

Test Step Dynamic Behaviour					
Test Step Name : S1_VERIFY					
Group : VERIFY/					
Objective : Procedure used to verify that the IUT is at state 1.					
Default :					
Comments :					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		(VR_MR:=GET_VR_MR())			
2		LT_PCO!BGAK	BGAK_S_GEN(VR_MR)		
3		START T_Wait			
4	LB1	LT_PCO?ENDPDU CANCEL T_Wait	END_R_SSCOP	(P)	IUT was at state 1
5		LT_PCO?UD	UD_R_GEN		
6		GOTO LB1			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		+TS_Wait			
Detailed Comments					

Test Step Dynamic Behaviour					
Test Step Name : S2_VERIFY					
Group : VERIFY/					
Objective : Procedure used to verify that the IUT is at state 2.					
Default :					
Comments :					
Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
2		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		VR(SQ)<>N(SQ)
3		START T_Wait			
4	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR)) CANCEL T_Wait	BGAK_R_GEN	(P)	IUT was at state 2
5		LT_PCO?UD	UD_R_GEN		
6		GOTO LB1			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		+TS_Wait			
Detailed Comments					

Test Step Dynamic Behaviour

Test Step Name: S4_VERIFY

Group : VERIFY/

Objective : Procedure used to verify that the IUT is at state 4.

Default :

Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		(VR_MR:=GET_VR_MR())			
2		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		VR(SQ)=N(SQ)
3		START T_Wait			
4	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR))	BGAK_R_GEN		
5		START T_Wait			
6	LB2	LT_PCO?ENDPDU CANCEL T_Wait	END_R_GEN	(P)	IUT was at state 4
7		LT_PCO?UD	UD_R_GEN		
8		GOTO LB2			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB2			
11		+TS_Wait			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?MD	MD_R_GEN		
15		GOTO LB1			
16		LT_PCO?ENDPDU	END_R_USER		
17		GOTO LB1			
18		+TS_Wait			

Detailed Comments

Test Step Dynamic Behaviour

Test Step Name: S5_VERIFY

Group : VERIFY/

Objective : Procedure used to verify that the IUT is at state 5.

Default :

Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		(VR_MR:=GET_VR_MR())			
2		LT_PCO!BGN	BGN_S_GEN(VT_SQ,VR_MR)		VR(SQ)=N(SQ)
3		START T_Wait			
4	LB1	LT_PCO?BGAK(VT_MS:=BIT_TO_INT(BGAK.N_MR)) CANCEL T_Wait	BGAK_R_GEN		
5		START T_Wait			
6	LB2	LT_PCO?RS(VR_SQ:=BIT_TO_INT(RS.N_SQ), VT_MS:=BIT_TO_INT(RS.N_MR)) CANCEL T_Wait	RS_R_RET(VR_SQ, VT_MS)	(P)	IUT was at state 5
7		LT_PCO?UD	UD_R_GEN		
8		GOTO LB2			
9		LT_PCO?MD	MD_R_GEN		
10		GOTO LB2			
11		+TS_Wait			
12		LT_PCO?UD	UD_R_GEN		
13		GOTO LB1			
14		LT_PCO?MD	MD_R_GEN		
15		GOTO LB1			
16		+TS_Wait			

Detailed Comments

Test Step Dynamic Behaviour

Test Step Name : S7_VERIFY
Group : VERIFY/
Objective : Procedure used to verify that the IUT is at state 7.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		(VT_SQ:=INC_MOD_8(VT_SQ,1), VR_MR:=GET_VR_MR())			
2		LT_PCO!ER	ER_S_GEN(VT_SQ,VR_MR)		VR(SQ)<>N(SQ)
3		START T_Wait			
4	LB1	LT_PCO?ERAK(VT_MS:=BIT_TO_INT(ERAK.N_MR)) CANCEL T_Wait	ERAK_R_GEN	(P)	IUT was at state 7
5		LT_PCO?UD	UD_R_GEN		
6		GOTO LB1			
7		LT_PCO?MD	MD_R_GEN		
8		GOTO LB1			
9		+TS_Wait			

Detailed Comments

Test Step Dynamic Behaviour

Test Step Name : S10_VERIFY
Group : VERIFY/
Objective : Procedure used to verify that the IUT is at state 10.
Default :
Comments :

Nr	Label	Behaviour Description	Constraints Ref	Verdict	Comments
1		(VT_PS:=INC_MOD_24(VT_PS,1))			
2		LT_PCO!POLL	POLL_S_GEN(VT_PS,VT_S)		
3		START T_Wait			
4	LB1	LT_PCO?STAT(VT_MS:=BIT_TO_INT(STAT.N_MR)) CANCEL T_Wait	STAT_R_N_R_S10_Verify(VT_PS)	(P)	
5		LT_PCO?POLL	POLL_R_GEN		
6		GOTO LB1			
7		?TIMEOUT T_Wait		(F)	
8		+postamble			

Detailed Comments