AK4324

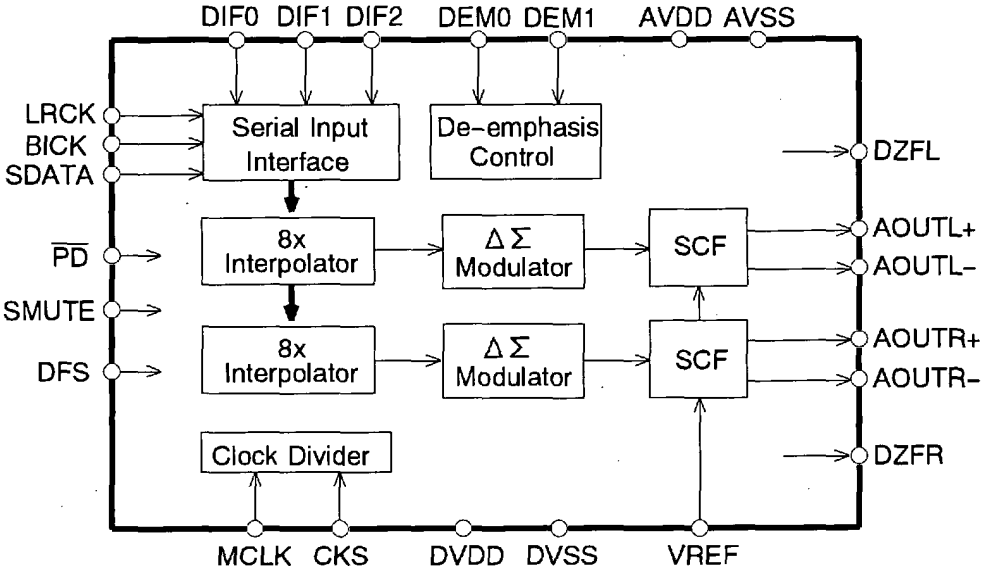
96kHz Sampling 24Bit ΔΣ DAC

General Description

The AK4324 is a high performance 1bit stereo DAC for the 96kHz sampling mode of DAT,DVD including a 24bit digital filter. A 1bit DAC can achieve monotonicity and low distortion with no adjustment and is superior to traditional R-2R ladder based DACs. In the AK4324, the analog outputs are filtered in the analog domain by switched-capacitor filter(SCF) with high tolerance to clock jitter. The digital I/F can correspond to TTL levels.

Features

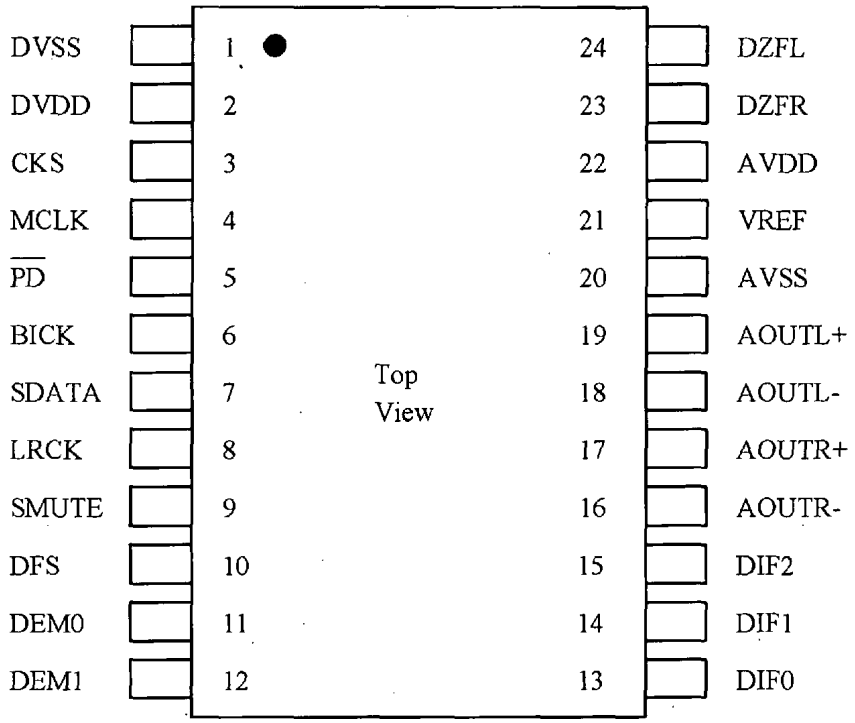
- ☐ High Performance Stereo 1bit DAC
- ☐ 128x Oversampling
- ☐ Sampling Rate up to 96kHz
- ☐ 24Bit 8 times Digital Filter
  - Ripple: ±0.005dB, Attenuation: 75dB
- ☐ 2nd Order SCF(LPF) with High Tolerance to Clock Jitter
- ☐ Low Distortion Differential Output
- ☐ Digital de-emphasis for 32, 44.1, 48kHz, 96kHz sampling
- ☐ Soft Mute
- ☐ I/F format : MSB justified, LSB justified, I2S
- ☐ Dynamic Range: 105dB
- ☐ Master Clock
  - Normal speed: 256fs or 384fs, Double speed: 128fs or 198fs
- ☐ Power Supply: 4.5 to 5.5V
- ☐ Small Package: 24pin VSOP



■ Ordering Guide

AK4324-VF	-40~+85°C	24pin VSOP(0.65mm pitch)
AKD4324	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	DVSS	-	Digital Ground Pin
2	DVDD	-	Digital Power Supply
3	CKS	I	Master Clock Select Pin (Internal Pull-down pin) Normal Speed #"L": MCLK=256fs, #"H": MCLK=384fs Double Speed #"L": MCLK=128fs, #"H": MCLK=192fs
4	MCLK	I	Master Clock Input Pin
5	$\overline{PD}$	I	Power-Down Mode Pin When at "L", the AK4324 is in power-down mode and is held in reset. The AK4324 should always be reset upon power-up.
6	BICK	I	Audio Serial Data Clock Pin 64fs clock is recommended to be input on this pin.
7	SDATA	I	Audio Serial Data Input Pin 2's complement MSB-first data is input on this pin.
8	LRCK	I	L/R Clock Pin
9	SMUTE	I	Soft Mute Pin When this pin goes "H", soft mute cycle is initiated. When returning "L", the output mute releases.
10	DFS	I	Double speed sampling mode Pin (Internal Pull-down pin) "L": Normal Speed, "H": Double Speed
11	DEM0	I	De-emphasis Frequency Select Pin
12	DEM1	I	De-emphasis Frequency Select Pin
13	DIF0	I	Digital Input Format Pin
14	DIF1	I	Digital Input Format Pin
15	DIF2	I	Digital Input Format Pin
16	AOUTR-	O	Rch Negative analog output pin
17	AOUTR+	O	Rch Positive analog output pin
18	AOUTL-	O	Lch Negative analog output pin
19	AOUTL+	O	Lch Positive analog output pin
20	AVSS	-	Analog Ground pin
21	VREF	I	Voltage Reference Input Pin
22	AVDD	-	Analog Power Supply Pin
23	DZFR	O	Rch Zero Input Detect Pin
24	DZFL	O	Lch Zero Input Detect Pin

Note: All input pins except internal pull-down pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS,DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog Digital DVDD-AVDD	AVDD DVDD VDA	-0.3 -0.3 -	6.0 6.0 0.3	V V V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Input Voltage		VIND	-0.3	AVDD+0.3	V
Ambient Operating Temperature		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	V

Note: 1 . All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS,DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies:	Analog (Note 2) Digital	AVDD DVDD	4.5 4.5	5.0 5.0	5.5 AVDD	V V
Voltage Reference (Note 3)		VREF	2.5	-	AVDD	V

Notes:2. AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD.

3. Analog output voltage scales with the voltage of VREF.
AOUT(typ.@0dB)=(AOUT+)-(AOUT-)=±2.8Vpp*VREF/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS (fs=44.1kHz)

(Ta=25°C; AVDD,DVDD=5.0V; VREF=AVDD; fs=44.1kHz; BICK=64fs;
Signal Frequency=1kHz; 24bit Input Data; Measurement Bandwidth=10Hz~20kHz; $R_L \geq 5k\Omega$;
unless otherwise specified)

Parameter		min	typ	max	Units
Resolution				24	Bits
Dynamic Characteristics (Note 4)					
THD+N	0dB Output -20dB Output -60dB Output		-94 -81 -41	-88 - -	dB dB dB
Dynamic Range (-60dB Output, A weight) (Note5)		100	105		dB
S/N (A weight) (Note 6)		100	105		dB
Interchannel Isolation(1kHz)		100	110		dB
DC Accuracy					
Interchannel Gain Mismatch			0.15	0.3	dB
Gain Drift (Note 7)			20	-	ppm/°C
DC Accuracy					
Output Voltage (Note 8)		±2.66	±2.8	±2.94	Vpp
Load Resistance		5			kΩ
Output Current				300	uA
Power Supplies					
Power Supply Current Normal Operation ($\overline{PD}$="H") AVDD DVDD Power-Down-Mode ($\overline{PD}$="L") AVDD+DVDD (Note 9)			 43 6 10	 64 9 50	 mA mA uA
Power Dissipation (AVDD+DVDD) Normal Operation Power-Down-Mode (Note 9)			 245 50	 365 250	 mW uW
Power Supply Rejection (Note 10)			50		dB

Notes:
4. Measured by AD725C(SHIBASOKU). Averaging mode. Refer to the eva board manual.
5. 100dB at 16bit data and 105dB at 20bit data.
6. S/N does not depend on input bit length. 101dB at CCIR-ARM weighted.
7. The voltage on VREF pin is held +5V externally.
8. Full-scale voltage(0dB). Output voltage scales with the voltage of VREF pin.
   AOUT(typ.@0dB)=(AOUT+)-(AOUT-)=±2.8Vpp*VREF/5.
9. Power Dissipation in the power-down mode is applied with no external clocks
   (MCLK,BICK,LRCK held "H" or "L").
10. PSR is applied to AVDD,DVDD with 1kHz, 100mVpp. VREF pin is held +5V.

ANALOG CHARACTERISTICS (fs=96kHz)

(Ta=25°C; AVDD,DVDD=5.0V; VREF=AVDD; fs=96kHz; BICK=64fs;
Signal Frequency=1kHz; 24bit Input Data; Measurement Bandwidth=20Hz~40kHz; $R_L \geq 5k\Omega$;
unless otherwise specified)

Parameter		min	typ	max	Units
Resolution				24	Bits
Dynamic Characteristics (Note 11)					
THD+N	0dB Output -20dB Output -60dB Output		-92 -78 -38	-86 - -	dB dB dB
Dynamic Range (-60dB Output)	(Note 12)		98		dB
S/N	(Note 12)	93	98		dB
Interchannel Isolation(1kHz)		100	110		dB
DC Accuracy					
Interchannel Gain Mismatch			0.15	0.3	dB
Gain Drift	(Note 13)		20	-	ppm/°C
DC Accuracy					
Output Voltage	(Note 14)	±2.66	±2.8	±2.94	Vpp
Load Resistance		5			kΩ
Output Current				300	uA
Power Supplies					
Power Supply Current					
Normal Operation ($\overline{PD}$="H")					
AVDD			43	64	mA
DVDD			9	13	mA
Power-Down-Mode ($\overline{PD}$="L")					
AVDD+DVDD	(Note 15)		10	50	uA
Power Dissipation (AVDD+DVDD)					
Normal Operation			260	385	mW
Power-Down-Mode	(Note 15)		50	250	uW
Power Supply Rejection	(Note 16)		50		dB

Notes:
11. Measured by UPD(ROHDE&SCHWARZ). Refer to the eva board manual.
12. 105dB at 20kHz LPF & A-weighted
13. The voltage on VREF pin is held +5V externally.
14. Full-scale voltage(0dB). Output voltage scales with the voltage of VREF pin.
AOUT(typ.@0dB)=(AOUT+)-(AOUT-)=±2.8Vpp*VREF/5.
15. Power Dissipation in the power-down mode is applied with no external clocks
(MCLK,BICK,LRCK held "H" or "L").
16. PSR is applied to AVDD,DVDD with 1kHz, 100mVpp. VREF pin is held +5V.

FILTER CHARACTERISTICS(fs=44.1kHz)

(Ta=25°C; AVDD,DVDD=4.5V~5.5V; fs=44.1kHz; DFS="0"; DEM0="1",DEM1="0")

Parameter	Symbol	min	typ	max	Units
Digital Filter					
Passband ±0.01dB (Note 17)	PB	0		20.0	kHz
-6.0dB		-	22.05	-	kHz
Stopband (Note 17)	SB	24.1			kHz
Passband Ripple	PR			±0.005	dB
Stopband Attenuation	SA	75			dB
Group Delay (Note 18)	GD	-	27.2	-	1/fs
Digital Filter + SCF					
Frequency Response 0~20.0kHz		-	±0.2	-	dB

Note: 17. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.01dB), SB=0.546*fs.
18. The calculating delay time which occurred by digital filtering. This time is from setting the data of both channels to input register to the output of analog signal.

FILTER CHARACTERISTICS(fs=96kHz)

(Ta=25°C; AVDD,DVDD=4.5V~5.5V; fs=96kHz; DFS="1"; DEM0="1",DEM1="0")

Parameter	Symbol	min	typ	max	Units
Digital Filter					
Passband ±0.01dB (Note 19)	PB	0		43.5	kHz
-6.0dB		-	48.0	-	kHz
Stopband (Note 19)	SB	52.5			kHz
Passband Ripple	PR			±0.005	dB
Stopband Attenuation	SA	75			dB
Group Delay (Note 20)	GD	-	27.2	-	1/fs
Digital Filter + SCF					
Frequency Response 0~40.0kHz		-	±0.3	-	dB

Note: 19. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.01dB), SB=0.546*fs.
20. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta=25°C; AVDD,DVDD=4.5~5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
High-Level Output Voltage (Iout=-100uA)	VOH	DVDD-0.5	-	-	V
Low-Level Output Voltage (Iout=100uA)	VOL	-		0.5	V
Input Leakage Current (Note 21)	Iin	-	-	±10	uA

Notes: 21 . DFS,CKS pins have internal pull-down devices, nominally 160kΩ.

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD,DVDD=4.5~5.5V; C_L=20pF)

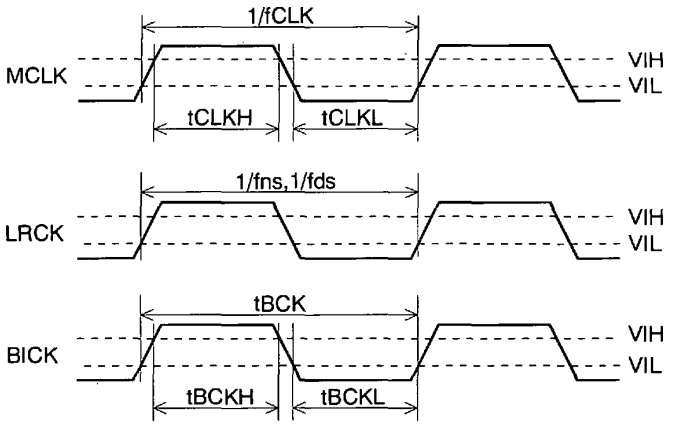
Parameter		Symbol	min	typ	max	Unit
Master Clock Timing	256fs:	fCLK	7.7		13.824	MHz
	Pulse Width Low	tCLKL	28			ns
	Pulse Width High	tCLKH	28			ns
	384fs:	fCLK	11.5		20.736	MHz
	Pulse Width Low	tCLKL	20			ns
	Pulse Width High	tCLKH	20			ns
LRCK Frequency	(Note 22)					kHz
Normal Speed Mode (DFS="L")		fsn	30	44.1	54	kHz
Double Speed Mode (DFS="H")		fsd	60	88.2	108	kHz
Duty Cycle		Duty	45		55	%
Serial Interface Timing						
BICK Period		tBCK	140			ns
BICK Pulse Width Low		tBCKL	60			ns
Pulse Width High		tBCKH	60			ns
BICK rising to LRCK edge	(Note 23)	tBLR	20			ns
LRCK Edge to BICK rising	(Note 23)	tLRB	20			ns
SDATA Hold Time		tSDH	20			ns
SDATA Setup Time		tSDS	20			ns
Reset Timing						
PD Pulse Width	(Note 24)	tPW	150			ns

Notes: 22. When the normal speed mode and the double speed mode are switched, AK4324 should be reset by PD pin.

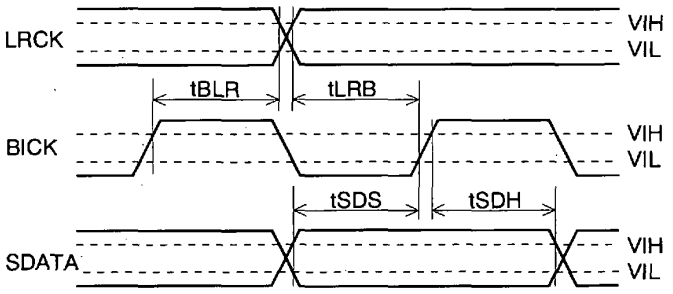
23. BICK rising edge must not occur at the same time as LRCK edge.

24. The AK4324 can be reset by bringing $\overline{PD}$ "L" to "H" only upon power up.

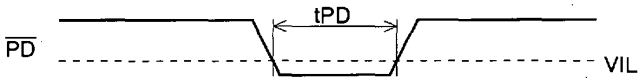
■ Timing Diagram



Clock Timing



Serial Interface Timing



Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks which are required to operate the AK4324 are MCLK, LRCK, BICK. The master clock(MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. The frequency of MCLK is determined by the sampling rate (LRCK), CKS pin and DFS pin. Table 1 illustrates corresponding clock frequencies. When the 384fs or 192fs is selected, the internal master clock becomes 256fs(=384fs*2/3) or 128fs(=192fs*2/3). Refer to Figure 1.

All external clocks(MCLK,BICK,LRCK) should always be present whenever the AK4324 is in normal operation mode($\overline{PD}$="H"). If these clocks are not provided, the AK4324 may draw excess current because the device utilizes dynamic refreshed logic internally. The AK4324 should be reset by $\overline{PD}$="L" after these clocks are provided. If the external clocks are not present, the AK4324 should be in the power-down mode($\overline{PD}$="L"). After exiting reset at power-up etc., the AK4324 is in power-down mode until MCLK and LRCK are input.

Speed		Normal(DFS="L")	Double(DFS="H")
LRCK (fs)		32k~48kHz	64k~96kHz
BICK		~64fs	~64fs
MCLK	CKS="L"	256fs	128fs
	CKS="H"	384fs	192fs

Table 1 . System Clocks

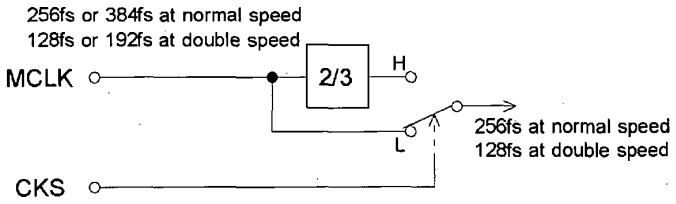


Figure 1 . MCLK divider at normal speed mode

■ Audio Serial Interface Format

Data is shifted in via the SDATA pin using BICK and LRCK inputs. Five serial data modes are supported and selected by the DIF0, DIF1 and DIF2 pins as shown in Table 2 . In all modes the serial data is MSB-first, 2's compliment format and is clocked on the falling edge of BICK. Modes 0-3 are compatible with AK4321. Mode 2 can be used for 20 and 16 MSB justified formats by zeroing the unused LSBs.

DIF2	DIF1	DIF0	Mode	BICK	Figure
0	0	0	0: 16bit LSB Justified	≥32fs	Figure 2
0	0	1	1: 20bit LSB Justified	≥40fs	Figure 3
0	1	0	2: 24bit MSB Justified	≥48fs	Figure 4
0	1	1	3: I^2S Compatible	≥48fs	Figure 5
1	0	0	4: 24bit LSB Justified	≥48fs	Figure 3
1	0	1	Test Mode		
1	1	1	DZF output is invalid.		
1	1	1			

Table 2 . Serial Data Modes

*The use of 64fs clock is recommended as BICK.

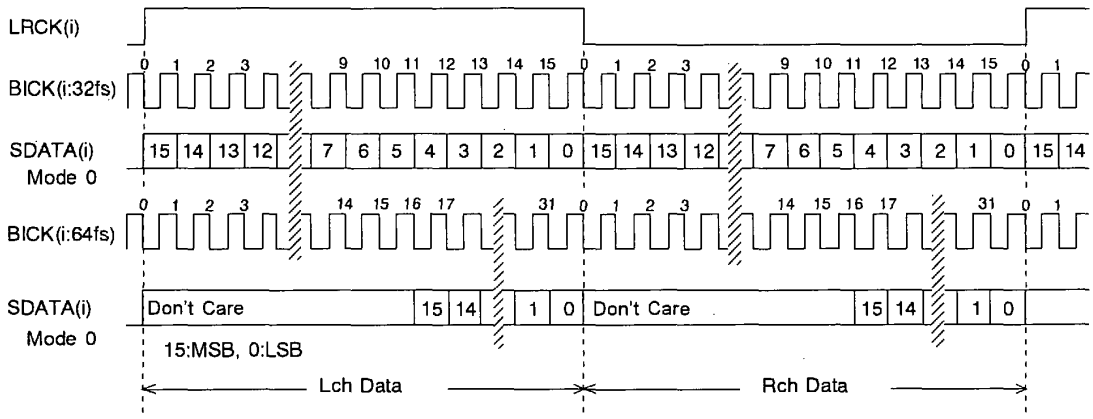


Figure 2 . Mode 0 Timing

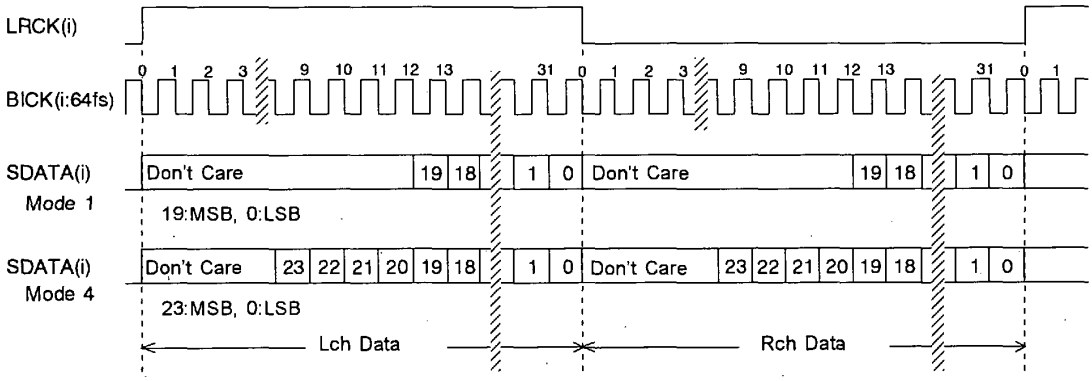


Figure 3 . Mode 1,4 Timing

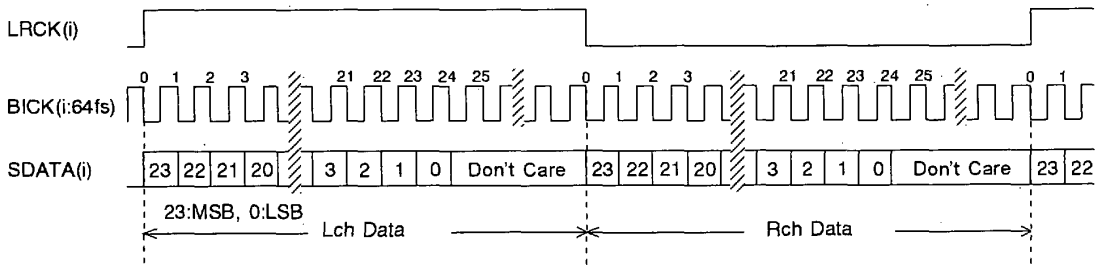


Figure 4 . Mode 2 Timing

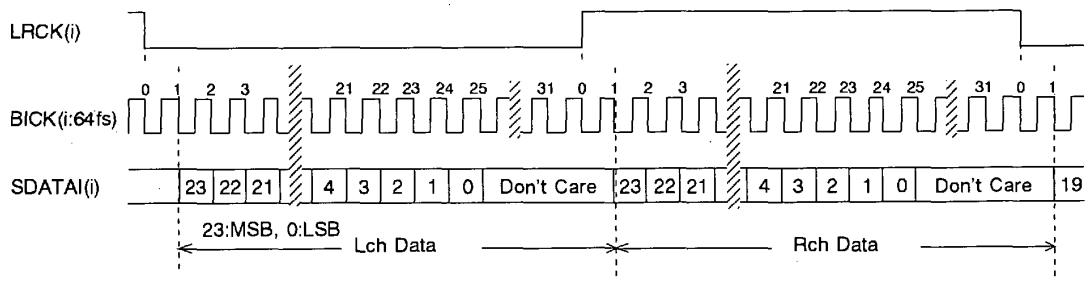


Figure 5 . Mode 3 Timing

■ **De-emphasis filter**

A digital de-emphasis filter is available for 32, 44.1, 48kHz or 96kHz sampling rates(tc=50/15us) and is enabled or disabled with the DEM0, DEM1 and DFS input pins.

DEM1	DEM0	DFS	Mode
0	0	0	44.1kHz
0	1	0	OFF
1	0	0	48kHz
1	1	0	32kHz
0	0	1	OFF
0	1	1	OFF
1	0	1	96kHz
1	1	1	OFF

Table 3 . De-emphasis filter control

■ **Zero detection**

The AK4324 has a channel separated zero detecting function. When the input data at left channel are continuously zeros for 8192 LRCK cycles, DZFL goes to "H". When the input data at right channel are continuously zeros for 8192 LRCK cycles, DZFR goes to "H". Each DZF immediately goes to "L" if input data are not zero after each DZF "H".
When the test mode in serial interface mode is enabled, the zero detection function is invalid.

■ **Soft mute operation**

Soft mute operation is performed at digital domain. When SMUTE goes to "H", the output signal is attenuated by -∞during 1024 LRCK cycles. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.

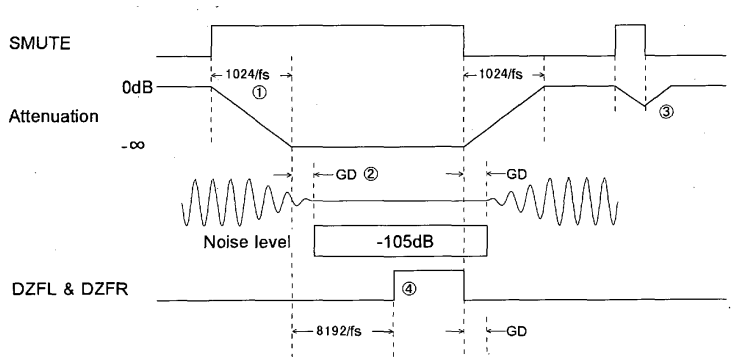


Figure 6 . Soft mute and zero detection

Notes:

① The output signal is attenuated by -∞ during 1024 LRCK cycles(1024/fs).

② Analog output corresponding to digital input have the group delay(GD).

③ If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.

④ As the input data at both channels are continuously zeros for 8192 LRCK cycles, both DZFs go to "H".
Both DZFs immediately go to "L" if input data are not zero after both DZFs "H".

■ **Power-Down**

The AK4324 are placed in the power-down mode by bringing $\overline{PD}$ pin "L" and the analog outputs are floating(Hi-Z). Figure 7 shows an example of the system timing at the power-down and power-up.

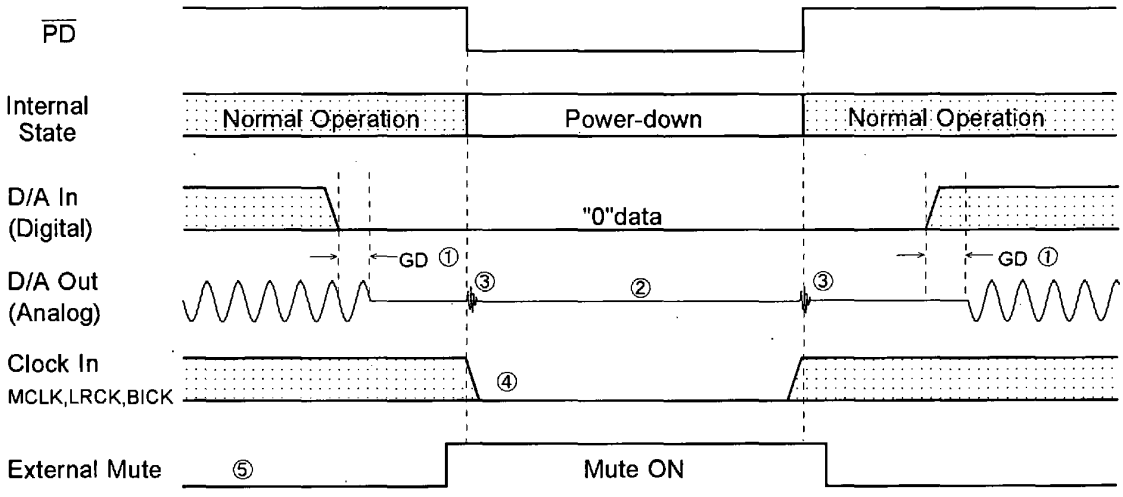


Figure 7 . Power-down/up sequence example

Notes:

① Analog output corresponding to digital input have the group delay(GD).

② Analog outputs are floating(Hi-Z) at the power-down mode.

③ Click noise about -50dB occurs at the edges("↑↓") of $\overline{PD}$ signal.
This noise is output even if "0" data is input.

④ When the external clocks(MCLK,BICK,LRCK) are stopped, the AK4324 should be in the power-down mode.

⑤ Please mute the analog output externally if the click noise(③) influences system application. The timing example is shown in this figure.

■ **System Reset**

The AK4324 should be reset once by bringing $\overline{PD}$ "L" upon power-up. The internal timing starts clocking by LRCK "↑" upon exiting reset by MCLK.

■ **Click Noise from analog output**

Click noise occurs from analog output in the following cases.

① When switching de-empahsis mode by DEM0,DEM1,DFS pins,

② When switching serial data mode by DIF0,DIF1,DIF2 pins,

③ When going and exiting power down mode by $\overline{PD}$ pin,

④ When switching normal speed and double speed by DFS pin,

However in case of ①& ②, If the input data is "0" or the soft mute is enabled (after 1024 LRCK cycles from SMUTE="H"), no click noise occur except for switching DFS pin.

SYSTEM DESIGN

Figure 8 shows the system connection diagram. An evaluation board[AKD4324] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

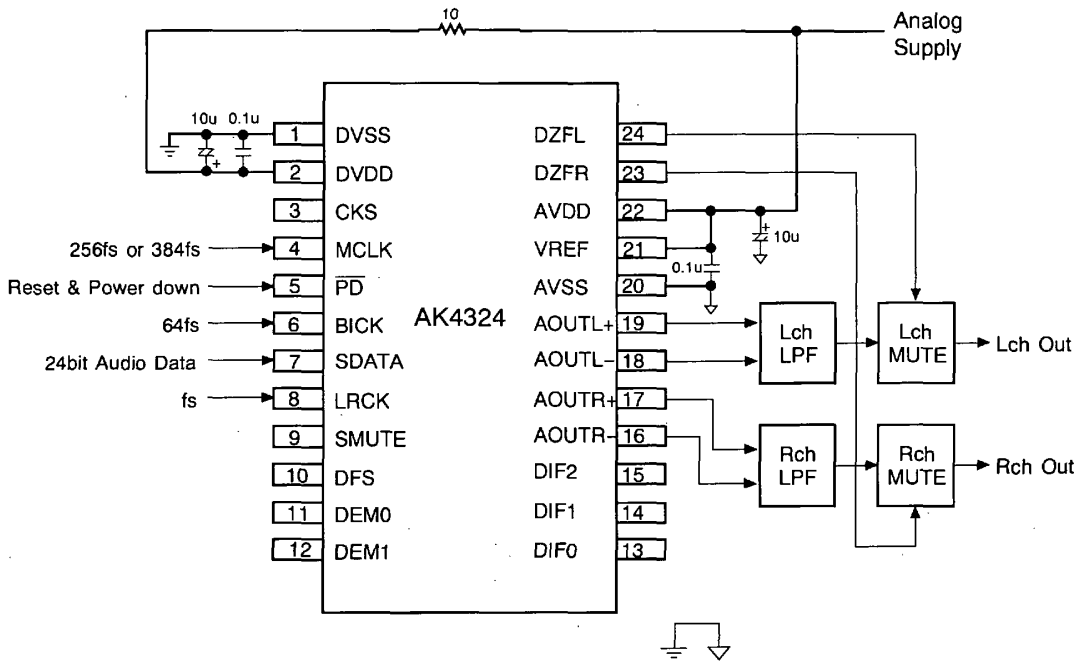


Figure 8 . Typical Connection Diagram

Notes:

- LRCK=fs, BICK=64fs.
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down pins(DFS,CKS) should not be left floating.

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from AVDD via 10Ω resistor. Alternatively if AVDD and DVDD are supplied separately, AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be placed as near as possible.

2. Voltage reference

The differential Voltage between VREF and AVSS set the analog output range. VREF pin is normally connected to AVDD with a 0.1uF ceramic capacitor. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the AK4324.

3. Analog Outputs

The analog outputs are full differential outputs and ±1.4Vpp(typ@VREF=5V) centered around AVDD/2. The differential outputs are summed externally, V_{AOUT}=(AOUT+)-(AOUT-) between AOUT+ and AOUT-. If the summing gain is 1, the output range is ±2.8Vpp(typ@VREF=5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage(V_{AOUT}) is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal V_{AOUT} is 0V for 000000H(@24bit).

The internal switched-capacitor filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. However, as the outband noise more than 40kHz is not so small in case of double sampling mode, some application may require external filter.

DC offset on analog outputs is eliminated by AC coupling since the differential outputs have DC offset of AVDD/2 + a few mV. Figure 9 shows the example of external op-amp circuit summing the differential outputs.

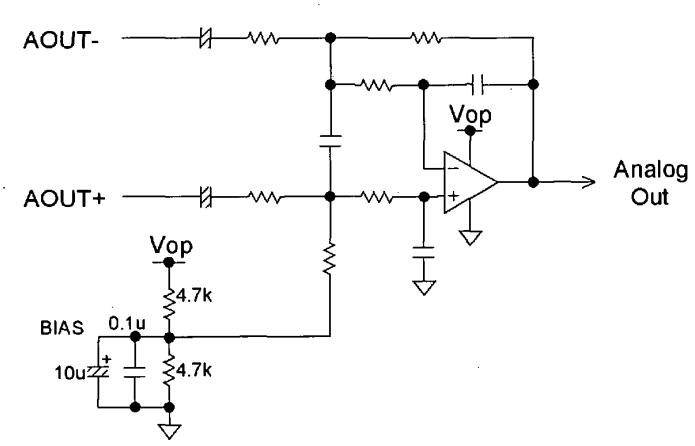
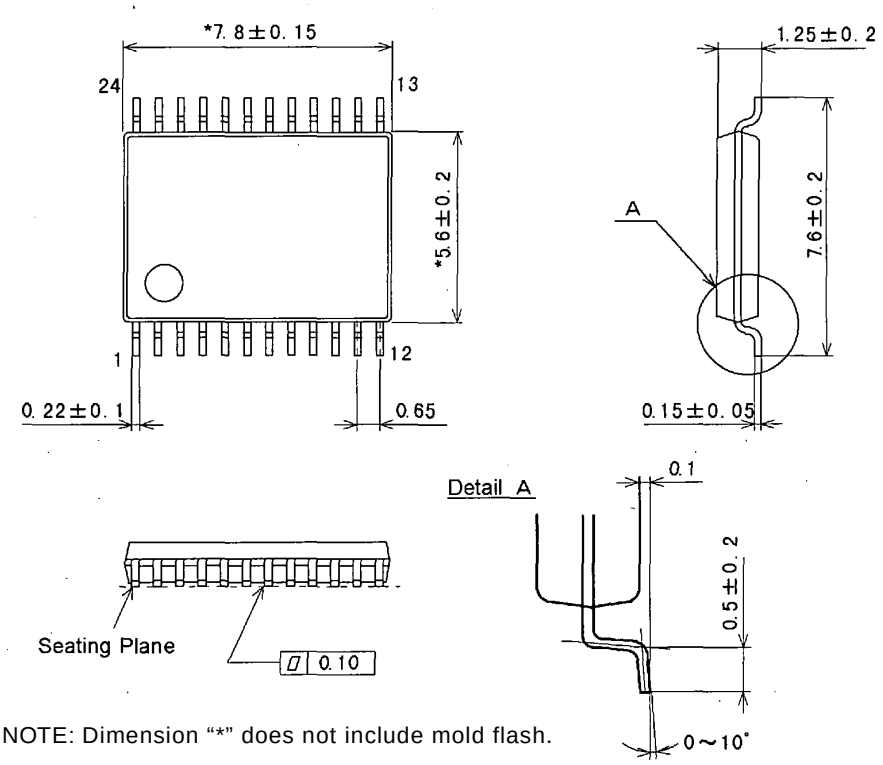


Figure 9 . External LPF Circuit Example

PACKAGE

● **24pin VSOP (Unit: mm)**

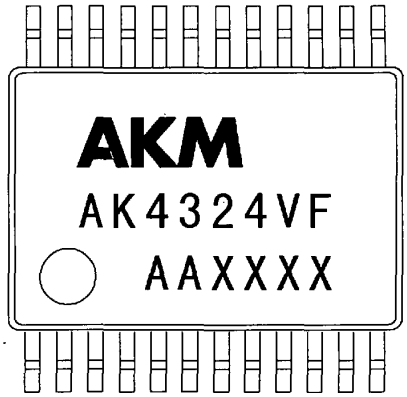


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



Contents of AAXXXX

AA: Lot#

XXXX: Date Code

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