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Peripheral Interface Controller Specification
Rev 1

1.0 Overview

The peripheral interface controller (PIC) is a custom IC designed to provide intelligent support for the SWIM disk controller or the Zilog 8530 Serial Communication Controller (SCC). The peripheral interface controller block diagram illustrates the major components of this chip. These components include a 65CX02 micro-processor operating at 2 MHz (ø2 frequency), one 16-bit timer, two DMA controllers, two digital phase locked loops (DPLL), and a RAM expansion bus accessible by the 65CX02 and the host processor.

The PIC is packaged in a 100 pin QFP.

1.1 Applicable Documents

For additional information about the features which the PIC supports refer to the documents listed below.

1. *NCR 65CX02 microprocessor data sheet*
2. *NCR Timer Supercell data sheet*
3. *Zilog 8530 SCC Technical manual*
4. *SWIM Chip Specification*

1.2 Host Processor Interface

The Host processor communicates with the PIC through an external static RAM IC which is time multiplexed between the two processors. A 16-bit auto-incrementing Address pointer register and an 8-bit data port allow the Host processor to access any location in the static RAM. In order to increase the 65CX02 instruction throughput, Host processor and DMA accesses to the RAM are performed during the unused 65CX02 ø2 clock low period. Arbitration priority for the RAM is fixed in the order of DMA channel 1, DMA channel 2, and finally the Host processor. The PIC can be configured with up to 60K bytes of off-chip static RAM.

1.2.1 SCC

Normally the PIC controls the SCC. However a special "Bypass" mode of operation is available in which the Host processor directly controls the SCC. This Bypass mode supplies a means of customizing the serial driver software for the SCC. The PIC controls the Bypass mode and thus the Host must make a request in order to gain control of the SCC. A bit in the Host status register (Address $2) monitors the SCC DMA request signal used by the serial driver software.

In the non-bypass mode of operation two DMA channels between the SCC and RAM offload the serial transactions from the 6502. DMA cycles are taken from the Host portion of the RAM cycle, thereby effectively reducing the Host RAM transfer rate. The minimum Host transfer rate, assuming a generic DMA device which forces DMA request always active, is 1MByte/sec. However with the SCC as the active DMA device receiving Appletalk data at 230.4KHz, the DMA request line will be asserted once every 35 usec, which reduces the effective Host RAM transfer rate from 2MBytes/sec to 1.97MBytes/sec.

Each DMA channel is controlled by a DMA transfer count register, DMA RAM address pointer, and DMA I/O address pointer.

1.2.2 DPLL

The PIC incorporates two digital phase locked loops (DPLL) for use with the SCC. The DPLL clock source is supplied externally via the PIC pin labeled DPCLK in order to permit the basic SDLC clock rate to be defined independently of the IOCLK frequency. Utilizing a DPCLK frequency of 20Mhz will generate 2Mbit LocalTalk data.

If the DPLL is enabled (Address $F032 bits D4,D6) then the DPCLK clock input is divided by 10 to obtain the phase locked loop frequency used for synchronizing with the incoming receive data. If valid receive data is not present on the incoming signal then the carrier sense bit in the DPLL control register (Address $F032, bits D5,D7) will be reset and the DPLL will enter the search mode. After entering the search mode the DPLL hunts for a clock edge. Once a clock edge is detected it is assumed to be valid and the carrier sense

bit is then set in the DPLL control register. The DPLL when locked then generates a clock which is synchronous but 90° out of phase with the incoming data.

To maintain a locked condition the DPLL utilizes an adjustment window which is ± 2 clocks on each side of the bit cell boundary. If an early receive data transition is detected within the adjustment window then the DPLL will remove one DPCLK clock from the synchronous receive clock, while if a late receive data transition is detected within the adjustment window then the DPLL will add one DPCLK clock to the synchronous receive clock. The DPLL expects to detect a valid edge during each bit cell period. If a clock is not present within the adjustment window during two consecutive bit cells then the DPLL will assume that synchronization has been lost and will reenter the search mode. The synchronous DPLL clock is enabled onto the SCC RTXC clock by setting the clock source bits in the PIC SCC/SWIM control register (Address $F030).

The DPLL is designed to synchronize on FM0 data. However in order to improve the SCC timing margins the incoming RXD FM0 data is recovered by the DPLL and converted to NRZ data which is then output on the RXDO pin. At the same time the DPLL generates an NRZ data recovery clock on the RTXC pin. This is the case whenever the DPLL enable bit is set in the PIC control register. In contrast if the DPLL enable bit is reset, then data on RXD is multiplexed directly onto the RXDO output. Consequently for serial modes which do not use the DPLL, there will be an additional timing delay in the receive data path. This delay is the PIC RXD to RXDO timing specification.

1.3 SWIM

The PIC is designed to be used either with the SCC or the SWIM. In order to accomplish this while still maintaining a reasonable package size, some of the PIC control lines differ between the two modes of operation. The control line changes are illustrated in the PIC schematic symbol diagrams and the PIC package diagram.

The timing for the SCC and the SWIM is different and this is under software control via the I/O delay/duration register (Address $F031). All other features of the PIC remain the same for both modes although some items such as interrupts are not supported by the SWIM. The SCC*/SWIM bit in the PIC control register (Address $F030 bit D1) selects which device the PIC interfaces with.

1.4 NCR Standard cells

The Timer Supercell and 65CX02 are elements of the NCR standard cell library. Both the timer and the 65CX02 operate at a 2MHz clock frequency. For additional information on the NCR cell library refer to the *NCR Semicustom Design data book.*

1.5 Signal Description

Inputs

DPCLK - Digital phase locked loop clock.
GPIA - General purpose input line from the channel A serial mini-DIN connector.
GPIB - General purpose input line from the channel B serial mini-DIN connector.
GPIN0 - General purpose input 0.
GPIN1 - General purpose input 1.
HA(0:4) - Address lines from the host processor.
/HCS0 - Active low chip select line from the host processor.
/HCS1 - Active low chip select line from the host processor.
HR/W - Read/write line from the host processor.
IOCLK - The 15.6672MHZ system clock. This clock operates the PIC state machines. It is also used to generate the 3.6864Mhz serial clock.
/PINT - The peripheral interrupt line.
/REQA - Active low channel A DMA request signal. (Active high DMA request signal from the SWIM).
/REQB - Active low channel B DMA request signal. (Active high DMA request signal from the SWIM).
/RESET - This active low signal resets the internal PIC registers and forces /PRD and /PWR low.
RXDA - Channel A receive data input. Used by the DPLL in order to construct a synchronous receive clock.
RXDB - Channel B receive data input. Used by the DPLL in order to construct a synchronous receive clock.
/TEST - Active low strobe used for enabling test modes.

Outputs

GPOUT0 - General purpose output 0.
GPOUT1 - General purpose output 1.
/HINT - open drain interrupt line to the host processor.
PA(0:3) - Address lines to the SCC/SWIM.
PCLK - The SCC PCLK. This signal has a clock frequency of DPCLK/2.
/PCS - Active low chip select line to the SCC/SWIM.
/PRD - Active low read line to the SCC.
/PWR - Active low write line to the SCC.
PR/W - Read/write line to the SWIM.

/RBCS - Active low chip select. This output decodes $F400-$F7FF.
/RCS - Active low chip select used to select external RAM. This output decodes memory locations $0000-$EFFF and $F800-$FFFF.
/ROE - Active low RAM output enable.
/RWE - Active low RAM write enable.
/RTXCA - SCC RTXC clock channel A. The PIC multiplexes either the GPIA input, the internal 3.6864Mhz clock, the DPCLK divided by 10, or the DPLL clock output onto this data line.
/RTXCB - SCC RTXC clock channel B. The PIC multiplexes either the GPIB input, the internal 3.6864Mhz clock, the DPCLK divided by 10, or the DPLL clock output onto this data line.
RXDAO - output to SCC RXD channel A. EIther the PIC RXDA input or the DPLL channel A NRZ data output are multiplexed onto this signal.
RXDBO - output to SCC RXD channel B. EIther the PIC RXDB input or the DPLL channel B NRZ data output are multiplexed onto this signal.
SYNC - Active during 65CX02 opcode fetches.
/TESTO - Test output.

Bidirectional

HD(0:7) - Host processor data bus.
/DSACK - Data strobe acknowledge to the host processor.
PD(0:7) - SCC/SWIM data bus.
R/W - 65CX02 read/write line. In test mode 3 this signal is used as a write enable input.
RA(0:15) - Multiplexed RAM address lines. In test mode 3 these signals are used as address inputs.
RD(0:7) - Multiplexed RAM data bus.
Ø2 - Normally the phase 2 output from the 65CX02. However, in test mode 1 this signal is used as the F2M input.

1.6 Test

The PIC test mode is enabled by strobing the /TEST, /HCS0, and /HCS1 inputs while writing the test number on the host data bus. The data value is latched into the PIC test register on the low to high transition of /TEST .

Loading the test register with a value of $0 selects the normal PIC mode of operation, while loading values $1-$3 select test modes 1 through 3 respectively. The test modes and their functions are described below.

Test Mode 1 (test register = $01) - This mode isolates the 65CX02 from all other PIC circuitry and allows a complete 65CX02 functional test to be executed. When this mode is selected the 65CX02 inputs and outputs are multiplexed onto the PIC pins as illustrated in the Test mode 1 pinout. 65CX02 signals are identified by the letter "P" followed by the NCR65CX02 supercell data sheet name. In addition to the 65CX02 signals, the host data bus and /TEST pins have been provided for test register access. This mode also is used to verify the DSACK watchdog timer. All other pin functions are undefined.

Test Mode 2 (test register = $02) - This mode places all of the PIC outputs in a high impedance state. Mode 2 is provided for Apple manufacturing.

Test Mode 3 (test register = $03) - This mode disables the 65CX02 and allows the internal microprocessor address and data busses to be controlled from the external address and data bus. The multiplexed address lines RA(0:15) become address inputs while the RD(0:7) data bus is used for reading and writing data values to the internal registers. The direction of data transfer is controlled by the external 65CX02 R/W line which is mapped as an input.

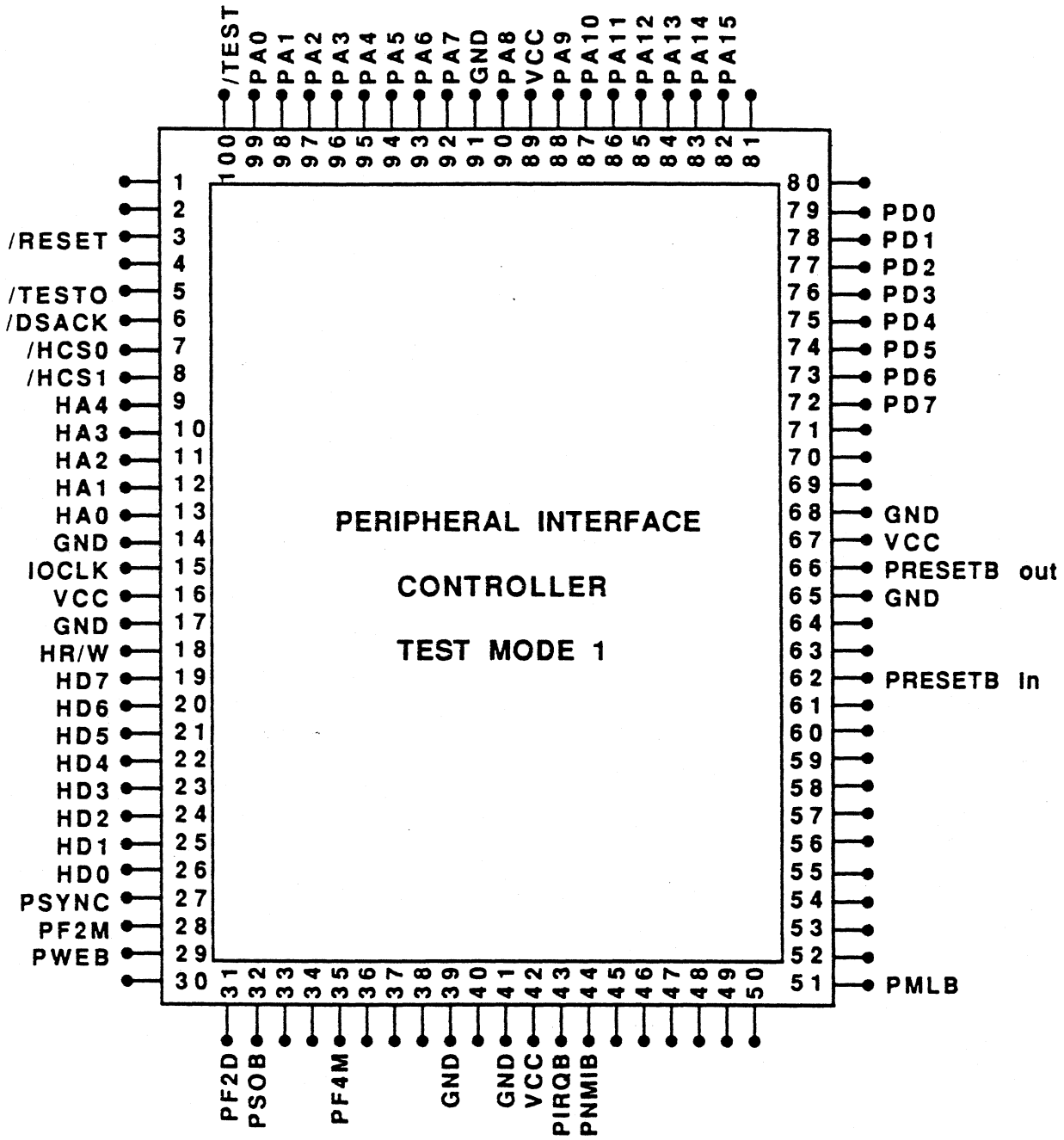

FIGURE 1.2 TEST MODE

1.8 AC Characteristics

Operating conditions unless otherwise noted: TA = 0 to 70 C, VCC = 4.5 to 5.5 V,
CL = 50 pf, Vref = 1.4 V.

Item	Description	Min	Max	Units	Notes
1	IOCLK frequency		16	Mhz	
2	IOCLK width high or low	20		ns	
3	Reset width	500		ns	
4	HA(0:4), HR/W setup to HCS0, HCS1 asserted	20		ns	
5	HA(0:4), HR/W hold from HCS0, HCS1 negated	0		ns	
6	HCS0, HCS1 asserted to HD(0:7) read data active	0		ns	
7	HD(0:7) read data valid to DSACK asserted	20		ns	1
8	HCS0, HCS1 negated to HD(0:7) read data invalid	0		ns	
9	HCS0, HCS1 negated to HD(0:7) read data high-Z		40	ns	
10	HCS0, HCS1 negated	30		ns	
11	HCS0, HCS1 asserted to HD(0:7) write data valid		60	ns	
12	HCS0, HCS1 negated to HD(0:7) write data invalid	0		ns	
13	HCS0, HCS1 negated to HD(0:7) write data high-Z		30	ns	
14	IOCLK high to DSACK asserted		38	ns	2
15	HCS0, HCS1 negated to DSACK negated		20	ns	2
16	HCS0, HCS1 negated to DSACK high-Z		42	ns	2
17	IOCLK high to RA(0:15) valid		55	ns	
18	RA(0:15) hold from RCS, ROE, RBCS negated	0		ns	
19	IOCLK high to RCS, RBCS valid		40	ns	
20	IOCLK high to ROE valid		40	ns	
21	RD(0:7) read data setup to IOCLK high	35		ns	
22	RD(0:7) read data hold from RCS, ROE, RBCS neg.	0		ns	
23	RD(0:7) read data high-Z from RCS, ROE negated		30	ns	
24	RD(0:7) write data valid to RWE, RBCS negated	100		ns	
25	RD(0:7) write data hold from IOCLK high	0		ns	
26	RD(0:7) write data high-Z from IOCLK high		50	ns	
27	IOCLK high to RWE valid		45	ns	
28	RWE width asserted	110		ns	
29	IOCLK high to F2M valid		38	ns	
30	F2M low to SYNC valid		55	ns	
31	F2M low to R/W valid		90	ns	
32	RA(0:15) hold from F2M low	0		ns	
33	RD(0:7) write data hold from F2M low	0		ns	
34	Asynchronous input setup to IOCLK high	30		ns	
35	Asynchronous input hold from IOCLK high	0		ns	
36	PCS asserted to REQn negated	0		ns	
37	REQn negated width	30		ns	
38	IOCLK high to PA(0:3), PR/W valid		65	ns	
39	IOCLK high to PCS valid		35	ns	
40	IOCLK high to PRD valid		40	ns	

41	PA(0:3), PR/W setup to PCS, PRD asserted	90		ns	
Item	Description Notes	Min	Max	Units	
42	PA(0:3), PR/W hold from PCS, PRD negated	0		ns	
43	PCS, PRD width asserted	T(n+1)		ns	3
44	PD(0:7) read data setup to IOCLK high	35		ns	
45	PD(0:7) read data hold from PCS, PRD negated	0		ns	
46	PD(0:7) read data high-Z from PCS, PRD negated		30	ns	
47	IOCLK high to PWR valid		35	ns	
48	PWR width asserted	T(n)		ns	3
49	IOCLK high to PD(0:7) write data valid		65	ns	
50	PD(0:7) write data valid to PWR asserted	25		ns	
51	PD(0:7) write data hold from PCS, PWR negated	0		ns	
52	PD(0:7) high-Z from PCS, PWR negated		20	ns	
53	DPCLK high to PCLK valid		45	ns	
54	IOCLK high to RTXCn valid		50	ns	
55	GPIn to RTXCn		35	ns	
56	DPCLK frequency		20	MHZ	
57	DPCLK high or low	20		ns	
58	DPCLK to RTXCn		50	ns	
59	Asynchronous input setup to DPCLK high	15		ns	
60	Asynchronous input hold from DPCLK high	15		ns	
61	IOCLK high to HINT asserted		65	ns	4
62	PINT asserted to HINT asserted		30	ns	4
63	DPCLK to RXDOn		35	ns	
64	GPIN0, GPIN1 setup to IOCLK high	40		ns	
65	GPIN0, GPIN1 hold from IOCLK high	0		ns	
66	IOCLK high to GPOUT0, GPOUT1		65	ns	
67	RXDn to RXDOn		25	ns	

Notes :

1 - HD(0:7) load CL=100pf
2 - DSACK load CL=100pf, 1Kohm pull-up to VCC
3 - T is IOCLK period in nanoseconds, n is the duration value in the I/O delay-duration register
4 - HINT load CL=50pf, 1.5Kohm pull-up to VCC

Sound Interface

The sound circuit consists of the Apple Sound Chip (ASC) and two Sony sound chips to filter the Pulse Width Modulated (PWM) signal and drive the on board speaker or external stereo miniphono jack. The DSC allows upward compatible sound generation with existing Macintosh software. The DSC adds two 1024 byte First-In-First-Out memories to accept the sound values instead of a single RAM address space. This removes much of the time critical nature of sound generation and gives stereo sound. In addition a four voice synthesis mode is a hardware implementation of the four voice driver in the Macintosh ROMs.

The DSC is further explained in "Apple Sound Chip (ASC), Pete Foley, 8-14-86".

The ASC has a byte wide data path into the chip. This means all normal accesses to the register set should be done with byte wide instructions. The FIFO RAM in the chip is a special case and can be loaded with long word instructions since the 68030 will automatically generate four byte accesses with incremented addresses. The use of long word aligned data in RAM and long word transfers into the ASC will result in minimal overhead for sound generation.

SWIM Interface

The Sander Woz Integrated Machine (SWIM) interface is the single chip that controls the one Sony floppy disk drive internal to the design and the one external. The SWIM contains shift registers to convert the bit steam from the drive to a byte stream to the processor. The SWIM is clocked by the C16M signal (15.6672 MHz) which is twice the frequency used in the original Macintosh. Thus the internal divide by two circuit must be used to access 800 K byte drives. When using Superdrives, the divide circuit will not be used.

Further information regarding the use of the SWIM can be found in "SWIM Chip Specification, Eric A. Baden, 9-29-1987". The signal interface from the 44 pin SWIM to the floppy disks is identical to the IWM in the Macintosh II. This includes the HDSEL signal from VIA1 which is used to select the drive head to allow software compatibility.

Table Floppy disk drive connectors

Pin #	Internal Connector-1&2	ribbon
1	GND	
2	PH0	
3	GND	
4	PH1	
5	GND	
6	PH2	
7	GND	
8	PH3	
9	no connect	
10	W/REQ	
11	+5 V	
12	HDSEL	
13	+12 V	
14	/ENABLE1	
15	+12 V	
16	RD	
17	+12 V	
18	WR	
19	+12 V	
20	no connect	

Apple DeskTop Bus Interface

Apple DeskTop Bus (ADB) is a serial communication bus used to connect keyboards, mice, graphics tablets, etc. to the computer, through the PIC chip. It is a single master multiple slave serial bus using an asynchronous protocol. The processor normally samples the state of each of the devices by using the control lines in VIA1 to read or write bytes to the Apple DeskTop Bus modem chip. This is a 4 bit microprocessor that actually drives the bus and reads the status of the selected device.

The protocol used to control the ADB modem is explained in **Apple DeskTop Bus Specification (Revision D)**, Bill Marino, 8-13-86, Apple Part # 062-0267.

The pinout for the ADB four pin Mini-DIN connector is shown in Figure 4.7.1. Pin 2 is used to allow the keyboard to power-on the power supply by shorting pins 2 and 4.

Table Apple DeskTop Bus Pins

Pin #	Comments
1	**Data.** This is the bi-directional data bus used for input and output. It is pulled up to +5 V through a 470 W resistor and is an open collector type signal.
2	**Power-On.** This signal is momentarily grounded to pin 4 to turn the power supply in the machine on. **No current draw is allowed.**
3	**Power.** This is +5V from the machine. A one amp fuse is in series with this output to satisfy the safety requirement.
4	**Return.** This is ground from the machine.

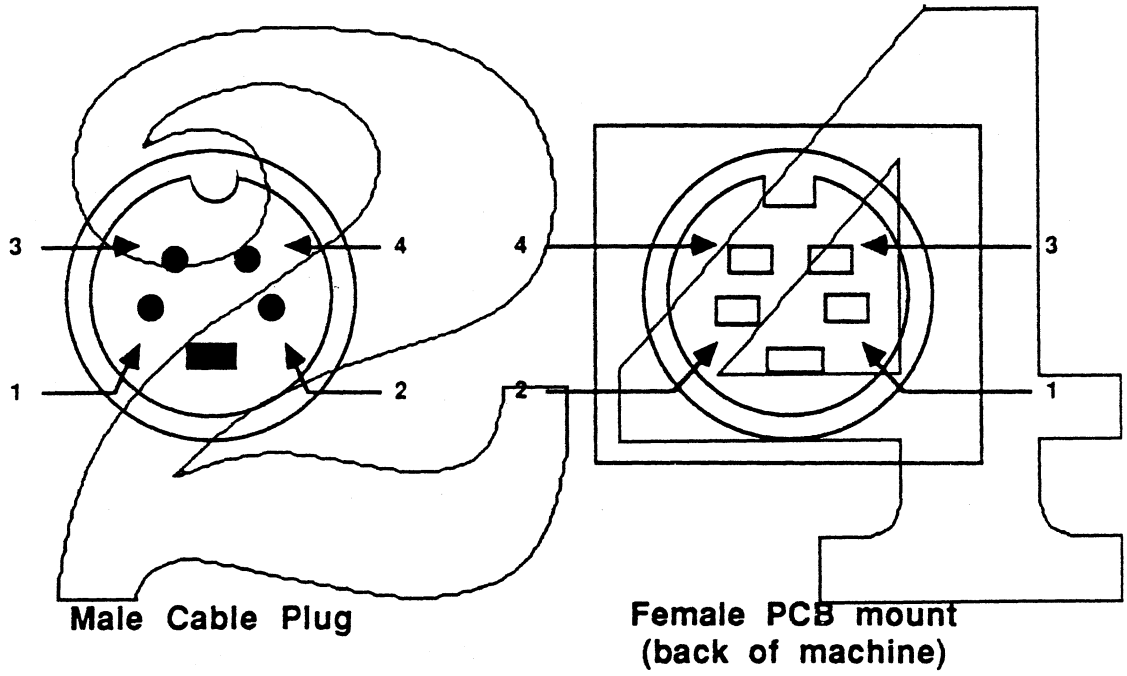

Figure 4.7.1Apple DeskTop Bus Mini-DIN 4 pin connector

"Soft" Power Control

The design has a 'Hard On/Soft Off' circuit to control the power supply. The circuit uses two 74HC132s, 3906 and 3904 transistors, and several capacitors and resistors. It is designed to control the power supply through the Power Fail Warning (PFW*) signal on NuBus.

The circuit is designed to attempt to turn on the power supply while the power switch is pressed and for 2 seconds after the power switch is pressed. The Apple DeskTop Bus keyboard has a secondary power switch which can turn on the machine. When the power switch is pressed it discharges a 0.22 mF capacitor through a 100 W resistor. The capacitor is charged through a 10M W resistor to the 5 volts supplied to the soft-power circuit, even when the computer is turned off, by the power supply. If AC current is present, the power supply will turn power on to the computer within 2 seconds. A diode and a 220 Ω resistor to +5V maintains current to the PFW* signal.

The power off function is under software control by using the menu command SHUTDOWN at the finder. This allows the computer to clean up any pending activity before power down. The power down switch generates a hard off that turns off the computer after 2 ms without going through software.

The poweroff 74HC132 is a Schmitt triggered set of NAND gates two of which are configured to form an SR flip-flop. When the processor is ready to power down the /POWEROFF signal from VIA2 is asserted which is connected to the /Set of the flip-flop, turning on the 3904, and pulling the PFW* signal to ground through a 27 ohm resistor. This causes the power supply to turn off after 2 ms. When the +5V power supply reaches 2 V the 3904 is turned off.